

AI Enhanced Physical Inspection for Counterfeit Microelectronics

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Genesis for Developing Secure Si-Interposers

**PSM – Ushering PCB Security Through System-
level MEMS Integration (N000142412056)**

PM Meeting – 19th May 2025



PSM Team

Program Managers ONR:

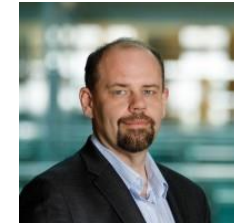
Dr. Ryan Craven

Dr. Daniel Koller

Task Leaders:

Dr. Navid Asadi (University of Florida)

Dr. Josh Hihath (Arizona State University)



Students:

Himanandhan Reddy K (Univ. of Florida ECE, Ph.D.)

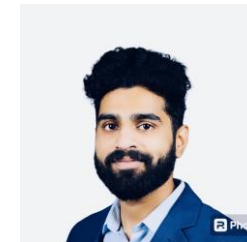
Pavanbabu (John) Arjunamahanthi (Univ. of Florida ECE, Ph.D.)

Shafkat Khan (Univ. of Florida ECE, Ph.D.)

Liam Hayes (Arizona State University ECE, Ph.D.)

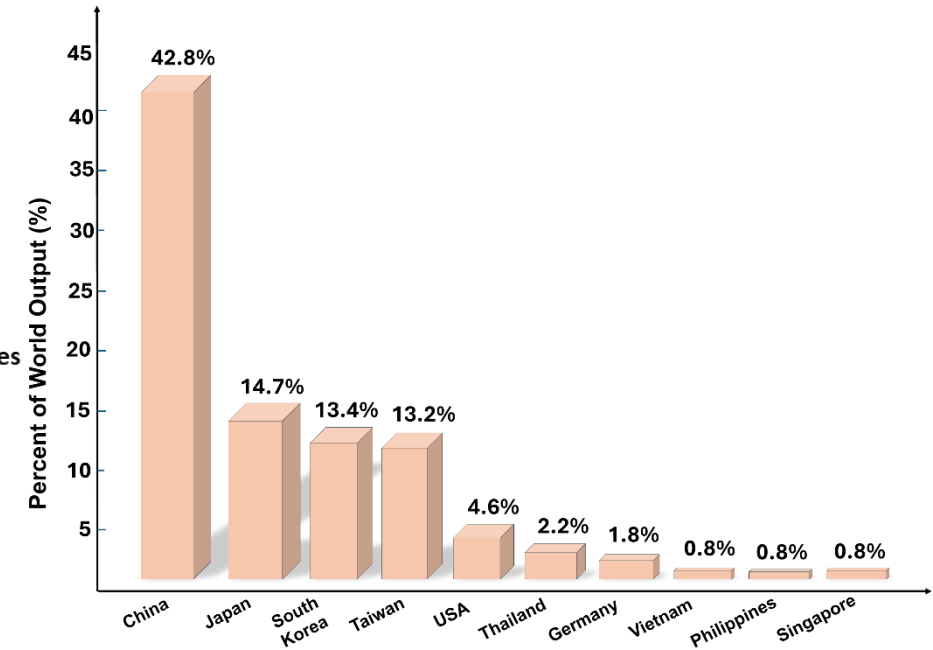
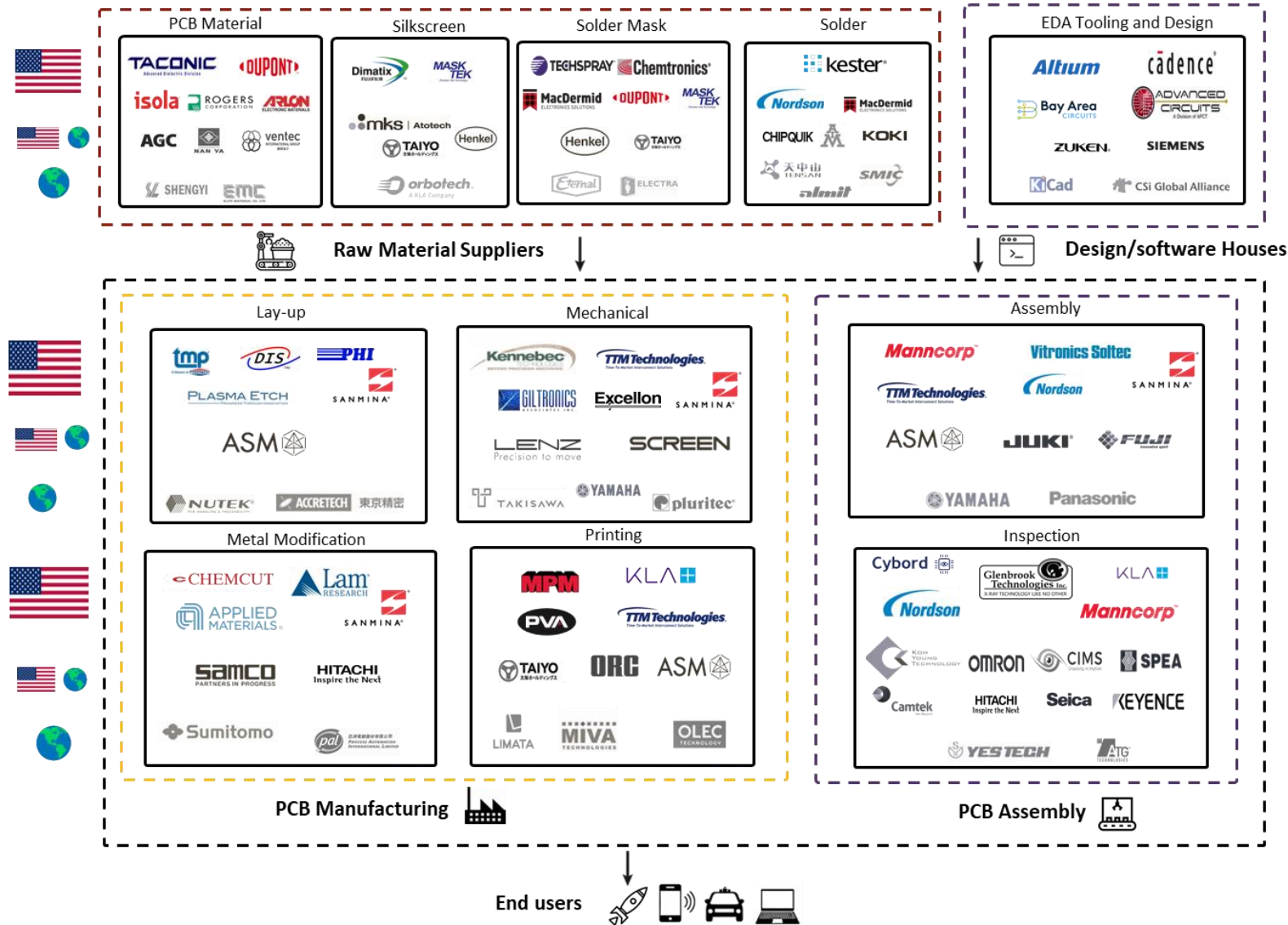
Kyoungdu Kim (Arizona State University ECE, Ph.D.)

Bo Liu (Arizona State University ECE, Post doc)



BACKGROUND

PCB Ecosystem and Market



- ✓ **Supply Chain:** Covers raw materials, PCB manufacturing, design, and assembly.
- ✓ **Key Players:** Includes DuPont, ASM, KLA, Nordson, etc.
- ✓ **Market Share:** Bar chart shows country wise production distribution.

The world map displays the global distribution of semiconductor manufacturing companies, categorized by technology type and region. The legend on the left identifies the categories:

- 3 manufacturers
- ries technology
- P technology
- O technology
- an-out technology manufacturers
- nology licensors
- R&D
- erging fan-out manufacturers

The map shows a high concentration of companies in Asia, particularly in South Korea, Taiwan, and Japan. Other significant clusters are found in North America and Europe. The map also includes labels for various companies and their locations, such as:

- North America:** INTEGRAL, Amkor technology, DECA, skywater, i3.
- Europe:** Fraunhofer, Infineon, Amkor technology, Formerly Nanium (Portugal), leti.
- Asia:** ASMeIT, SAMSUNG, SHINKO, ne:es, LB Semicon, Korea, Part of JCET, Amkor technology, Unimicron, INNOLUX, JCET, HUA TIAN, SPIL, a, ITRI, Powertech, OIP, SILICON BOX, ne:es, The Philippines, MST, DED, STI, Malaysia, Formerly Stats ChipPAC Singapore, JCET, JCAP China, Previously ESWIN, TSMC, ASE GROUP, TSMC, Unimicron, INNOLUX, JCET, HUA TIAN, SPIL, a, ITRI, Powertech, OIP, SILICON BOX, ne:es, The Philippines, MST, DED, STI, Malaysia, Formerly Stats ChipPAC Singapore.

Reference: Yole 2023

Scenarios – Real Time Attacks

Your Air Force

An F-16 pilot died when his ejection seat failed. Was it counterfeit?

By [Rachel S. Cohen](#) Sep 13, 2022

[f](#) [t](#) [r](#) [in](#) [g](#) [e](#)



David Schmitz, then a staff sergeant, poses in 2014 at Joint Base Lewis-McChord, Wash. (Jacob Jimenez/Air Force)

 Defense One

China's Copycat Jet Raises Questions About F-35

New technical specs about China's new J-31 fighter, a plane designed to rival the American-made F-35 Joint Strike Fighter, popped up on a Chinese blog last...



 IEEE Spectrum

Invasion of the Hardware Snatchers: Cloned Electronics Pollute the Market

Fake hardware could open the door to malicious malware and critical failures.



 Hackaday

iPhone 6S NVMe Chip Tapped Using A Flexible PCB

Psst! Hey kid! Want to reverse-engineer some iPhones? Well, did you know that modern iPhones use PCIe, and specifically, NVMe for their...



 The Aviationist

Iran unveils reverse-engineered version of captured U.S. RQ-170 stealth drone

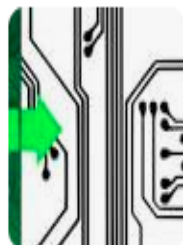
Iran unveiled an RQ-170 drone allegedly manufactured by reverse-engineering of US Sentinel drone captured in December 2011.



 Hackaday

Reverse Engineering A PCB

Occasionally when a device breaks, the defect is obvious. Whether it is a blown fuse or a defective capacitor, generally the easy to see...



RESEARCH APPROACH

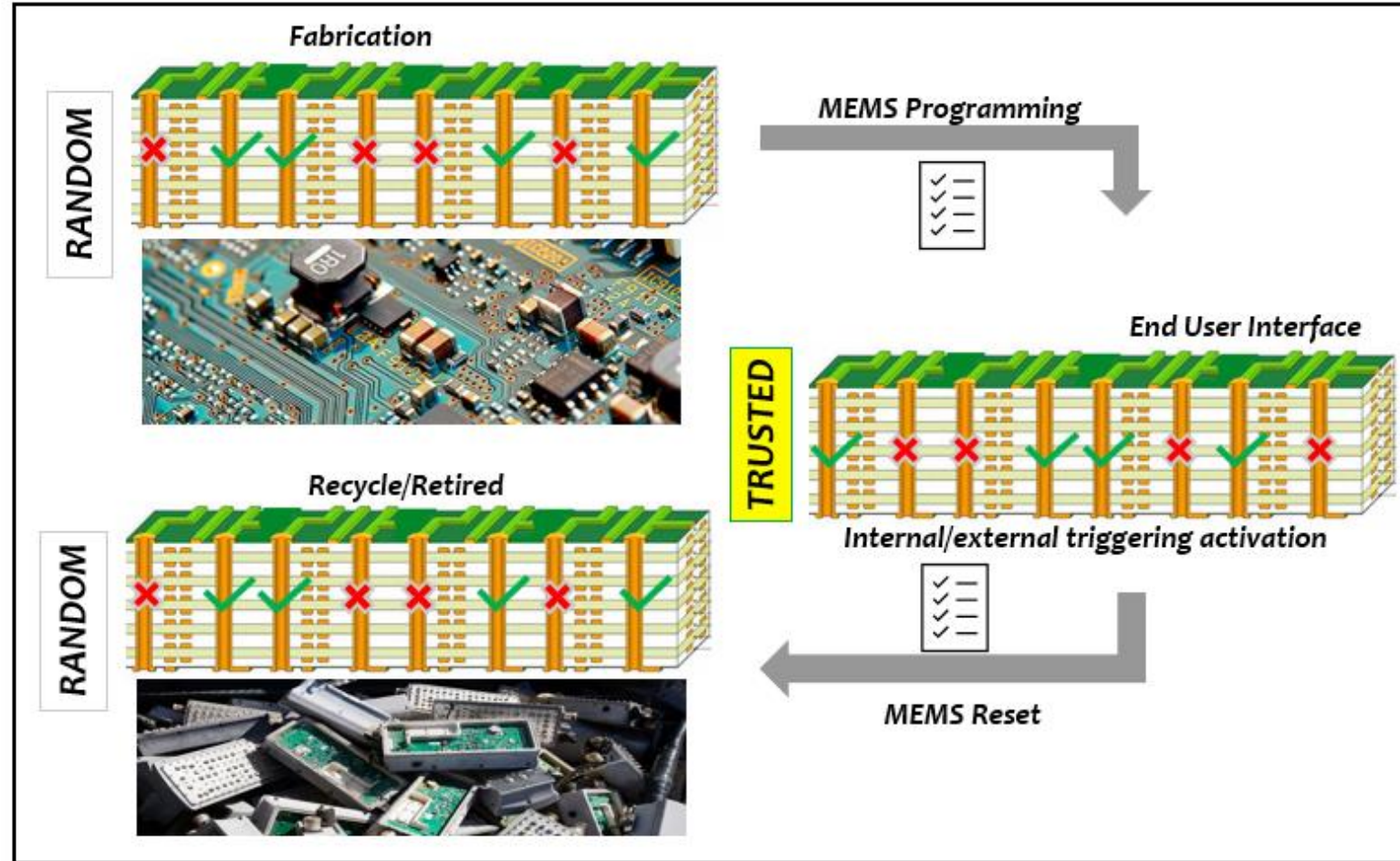
PSM Strategy

MEMS Switches
Configuration

Connected



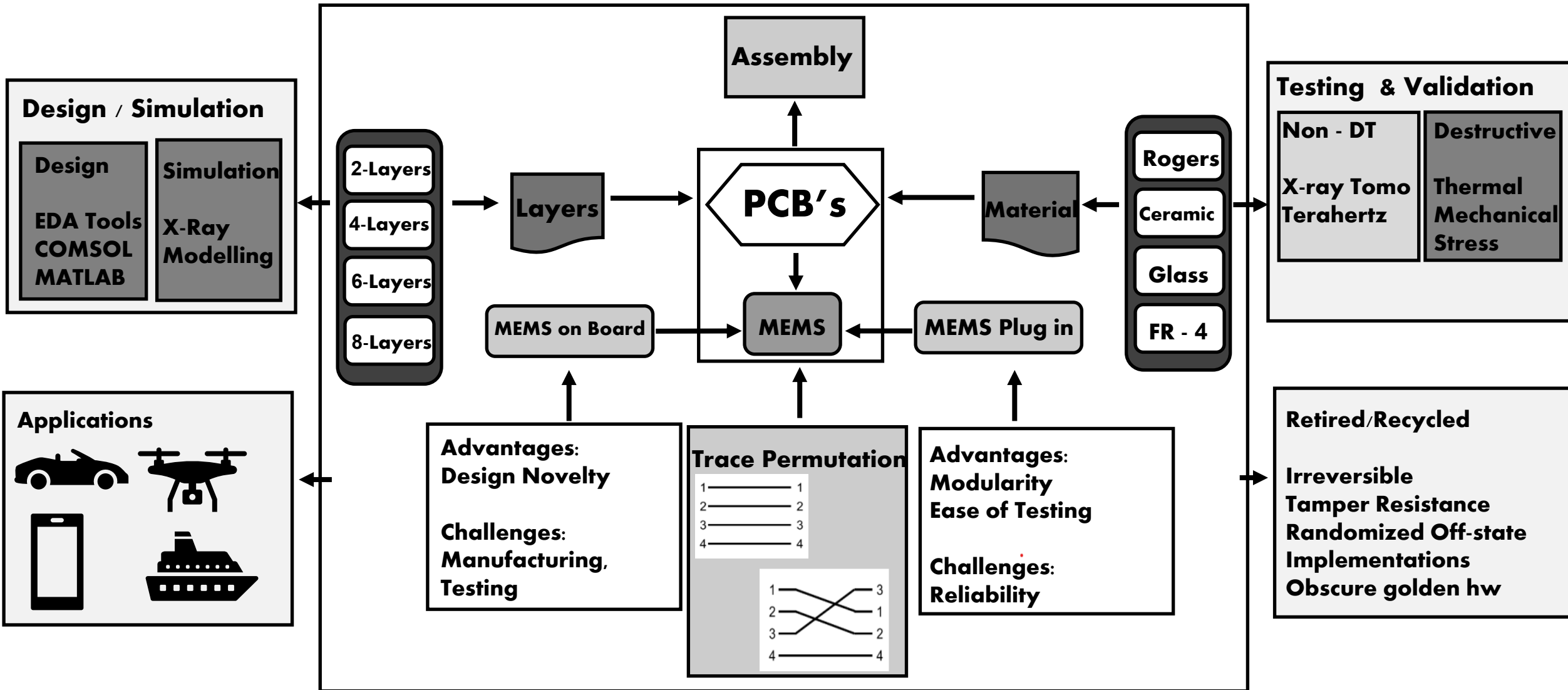
Disconnected



End Users

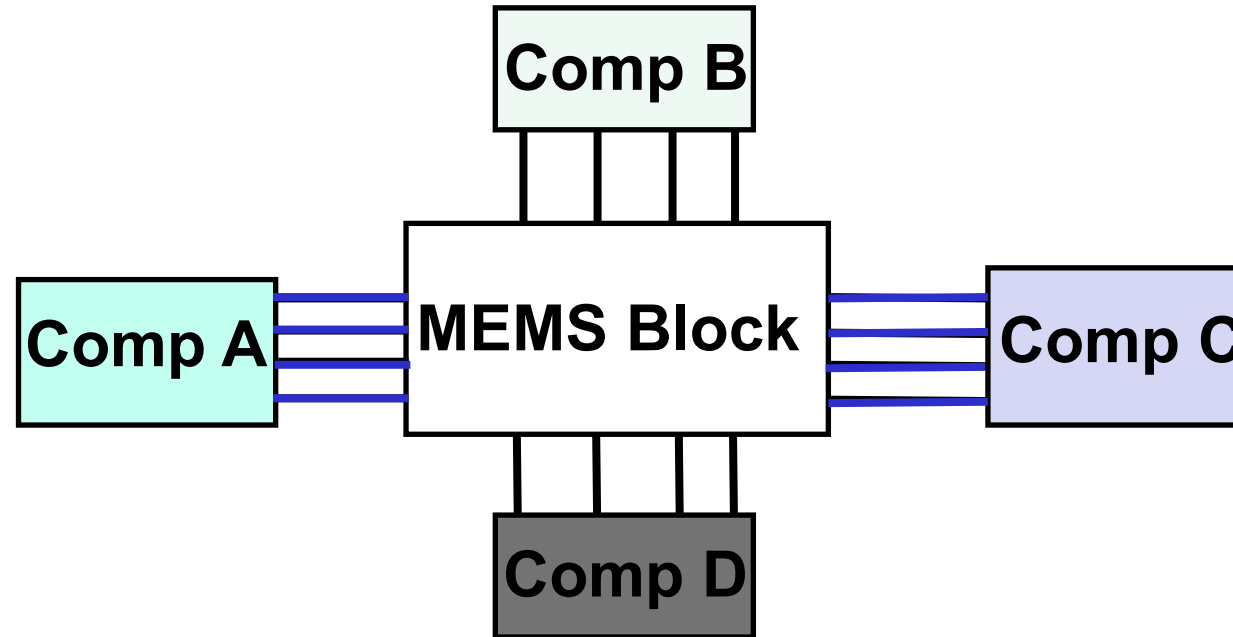


Solution Overview



Entropy Analysis – Case 1

 **Case 1: All 4 Traces Go to Only One Other Component at a Time**



Case 1:

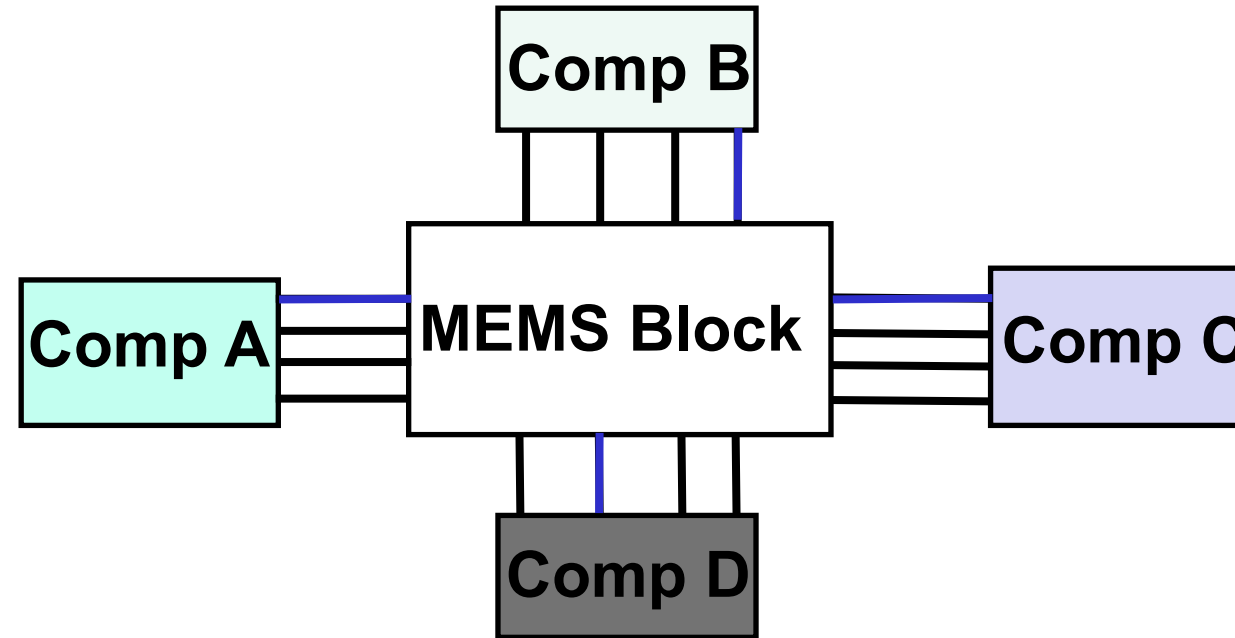
- ❑ Each component (e.g., Comp A) sends **all 4 traces** to just one of the remaining components (B, C, D).
- ❑ **3 destination choices** for each component.
- ❑ **4 traces** can be permuted in **$4! = 24$** ways.
- ❑ So, **total permutations per component** = $3 \times 24 = 72$.

For each of the 4 components independently

$$72^4 = \boxed{26,873,856 \text{ total permutations}}$$

Entropy Analysis – Case 2

✂ Case 2: Traces Can Be Split Across Multiple Components



Case 2:

- ❑ Each of the 4 traces can be routed independently to any of the 3 other components.
- ❑ **Routing combinations per component** = $3^4 = 81$
- ❑ For each combination, **trace-to-pad permutations** ≈ 24 (assumes typical distribution like 2 to B, 1 to C, 1 to D).
- ❑ So, **total permutations per component** = $81 \times 24 = 1,944$.

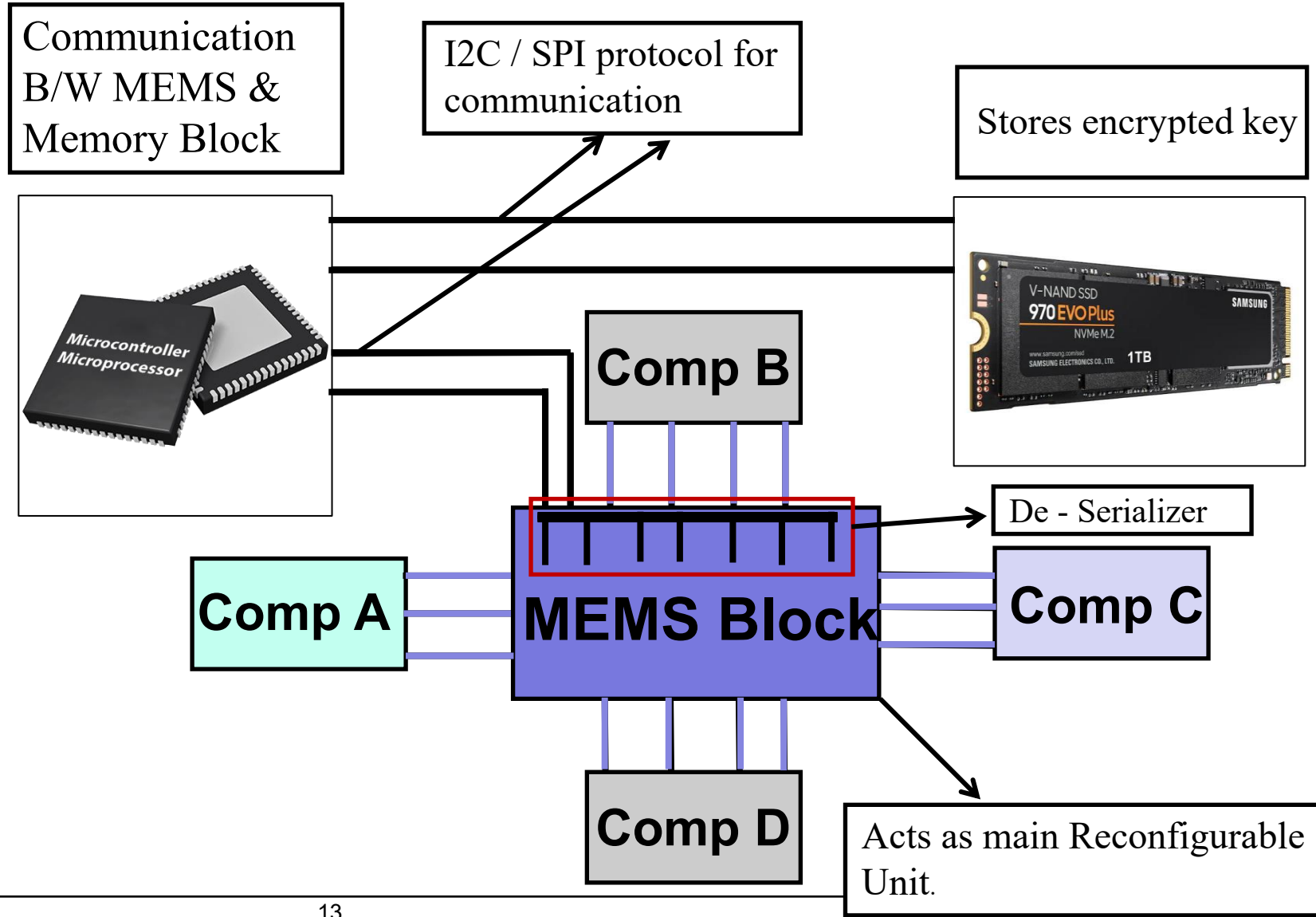
For each of the 4 components independently

$$1944^4 \approx 1.427 \times 10^{13} \text{ total permutations}$$

Key Communication Unit

Step by Step Process

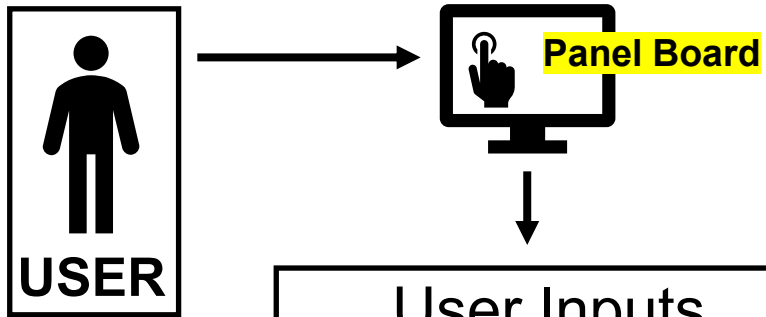
- **Power-Up:**
- Processor initializes and verifies the NVM integrity through digital certificate saved.
- **Key Retrieval:**
- The processor retrieves and decrypts the key securely.
- **Key Validation:**
- The MEMS block authenticates the key and configures accordingly.
- **Configuration:**
- MEMS block establishes secure communication pathways between components.



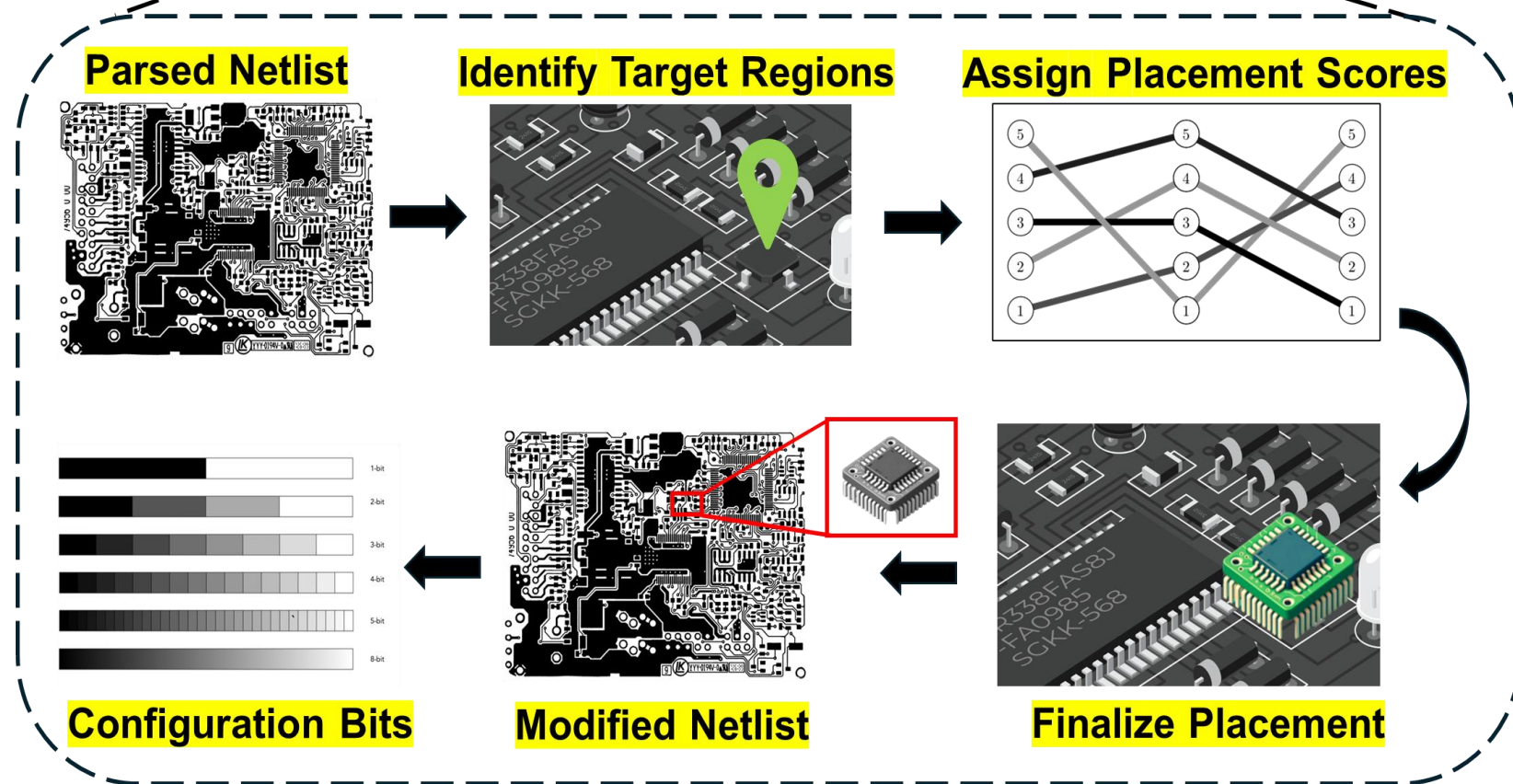
MEMS-Enabled PCB Security (MEPS) – Workflow



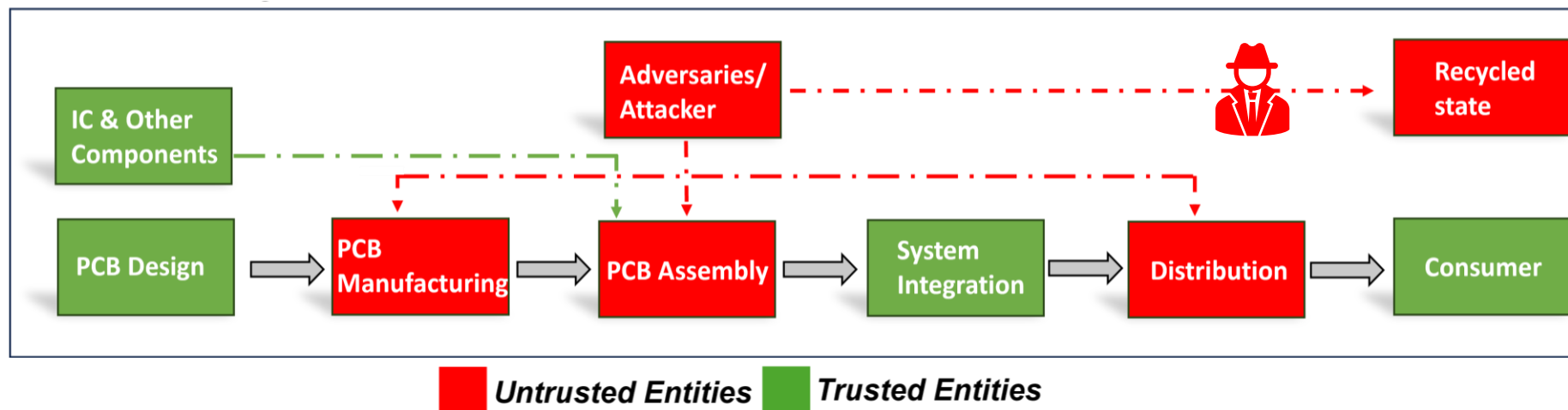
Constraints



- Pre-Obfuscated Netlist
- Priority Components
- No of MEMS Plug In
- Size of MEMS Plug Ins

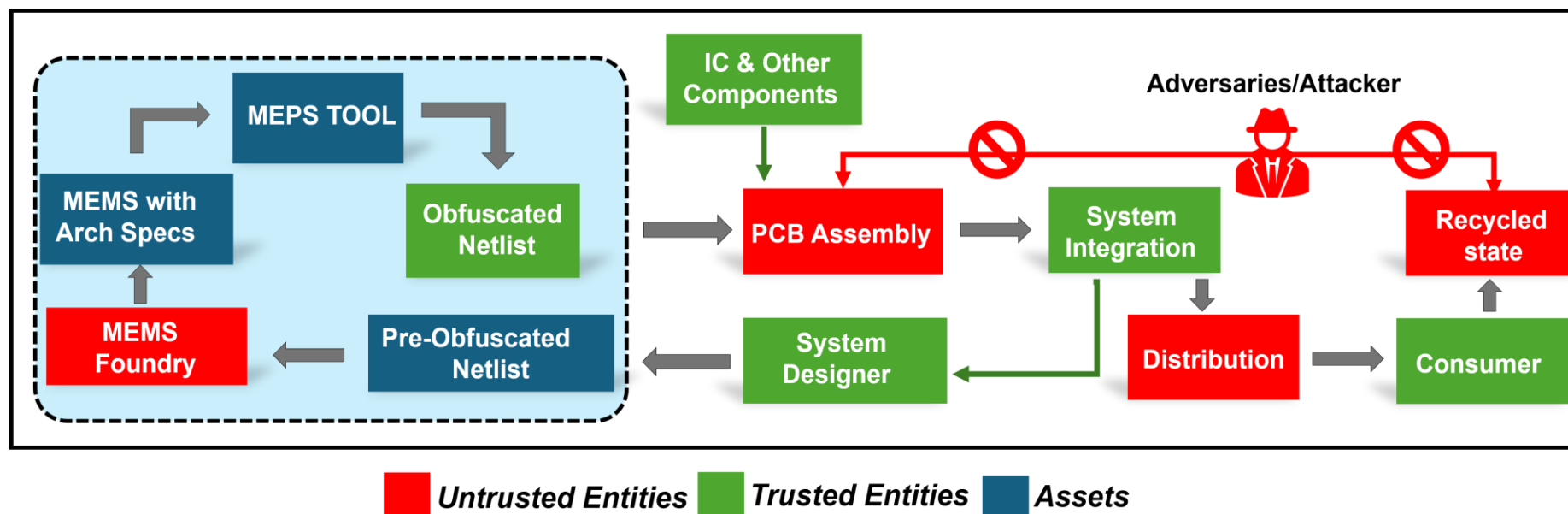


Supply Chain Before and After



Without MEPS

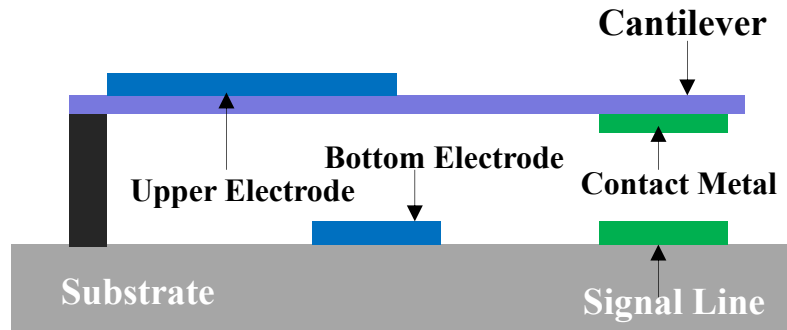
- Higher risk of tampering and counterfeiting.
- Predictable interconnects enable reverse engineering.
- Vulnerable end-of-life security.



With MEPS

- Unique MEMS arrays prevent replication.
- Reduced supply chain attack risks.
- Strong protection against reverse engineering.

MEMS Cantilever Beam Characteristics



for $L = 260 \mu\text{m}$, $w = 50 \mu\text{m}$, $h = 1 \mu\text{m}$ and $d_n = 1 \mu\text{m}$

Beam Material	Density (kg/m ³)	First natural frequency (kHz)
Polysilicon	2330	18.590
Aluminum	2700	258.03
Gold	19300	4.834

Component	Vibrational frequency
Submarine	10 – 200 Hz
Commercial aircraft	10 – 100 Hz
Military aircraft	10 – 2000 Hz
Medical devices (MRI)	20 – 100Hz

Table 1. Young's modulus and Poisson ratio for several materials

Material	Young's modulus (E) [GPa]	Poisson ratio (ν)
Polysilicon	141	0.27
Aluminum	70	0.33
Gold	79	0.44

$$\frac{d^2 y}{dx^2} = \frac{M}{EI}, \quad \Rightarrow \quad \text{Deflection of Cantilever beam}$$

Higher deflection

Undesirable properties:

- Increased contact resistance
- Material fatigues
- Stiction
- Electrical failures

Natural frequency Higher the gap Operating environment frequency ➔ Better performance

PSM proposed MEMS switch contains Aluminum, hence the optimal choice

Testing Methodologies

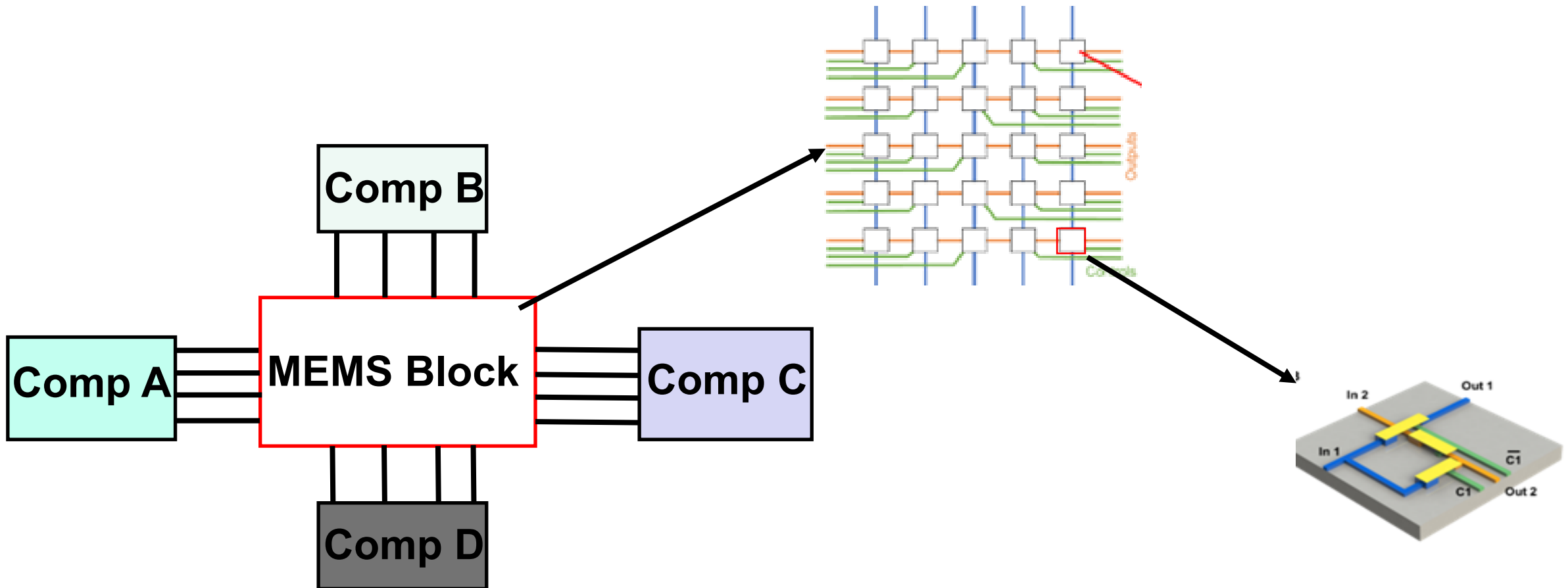
Tests	Details	Standards
Physical Inspection	Physical Inspection and Visual Check	ISO 9001:2015 – Quality management – Requirements. KGD
Electrical Characterization	Contact Resistance, Electrical Performance and Switching Performance Tests	MLF - PRF - 123 – Performance Specification Electronic Components, General Specification for, IEC 60512 – Connectors for Electronic Equipment Tests and Measurements, IEEE 1452 – Standard for a Smart Transducer Interface and Sensors and Actuators
Mechanical Characterization	Reliability and Durability Tests	IEC 60749 – Semiconductor Devices – Mechanical and Climatic Test Methods
	Temperature and Environmental Tests	MIL-STD-810 – Test Method Standard for Environmental Engineering Considerations and Laboratory Tests
	Vibration and Shock Resistance	IEC 60068-2 – Environmental Testing – Part 2: Tests, Test B: Dry Heat

Additional Testing Plans

Tests	Standards
Hermeticity and Packaging Tests	ASTM E2512 – Standard Test Method for Determination of Noise Equivalent Power (NEP) and Noise Equivalent Concentration (NEC) of a Photoacoustic Spectrometer
Calibration and Standardization	ISO/IEC 17025 – General Requirements for the Competence of Testing and Calibration Laboratories
Failure Modes and Reliability Tests	JEDEC, JESD22 – Series of standards for testing semiconductors devices, including mechanical and Environmental tests.

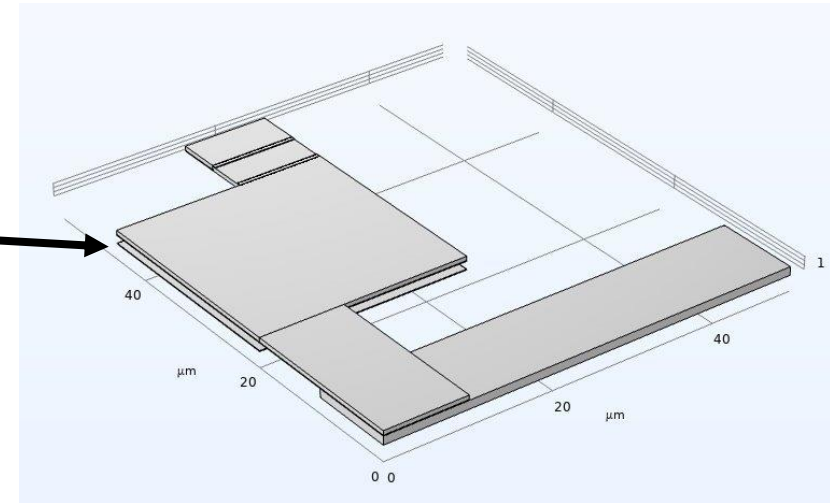
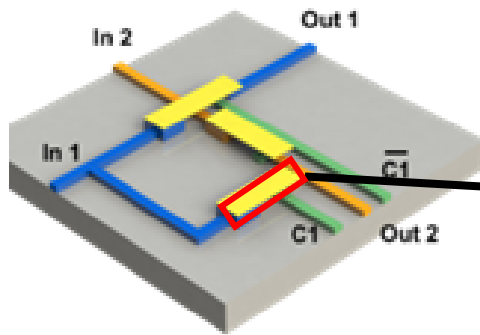
ASU Goals

- ❑ Design and Fabrication of MEMS block is critical to system level design
- ❑ Within each MEMS block, switching cells are present
- ❑ MEMS cantilever switches are the critical devices within each cell



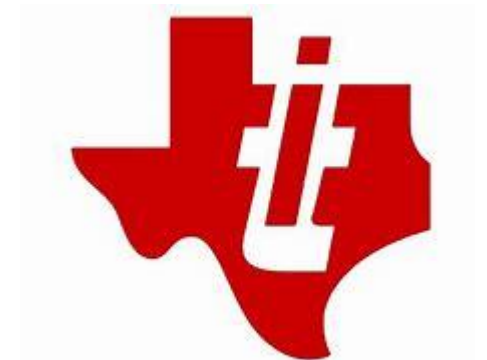
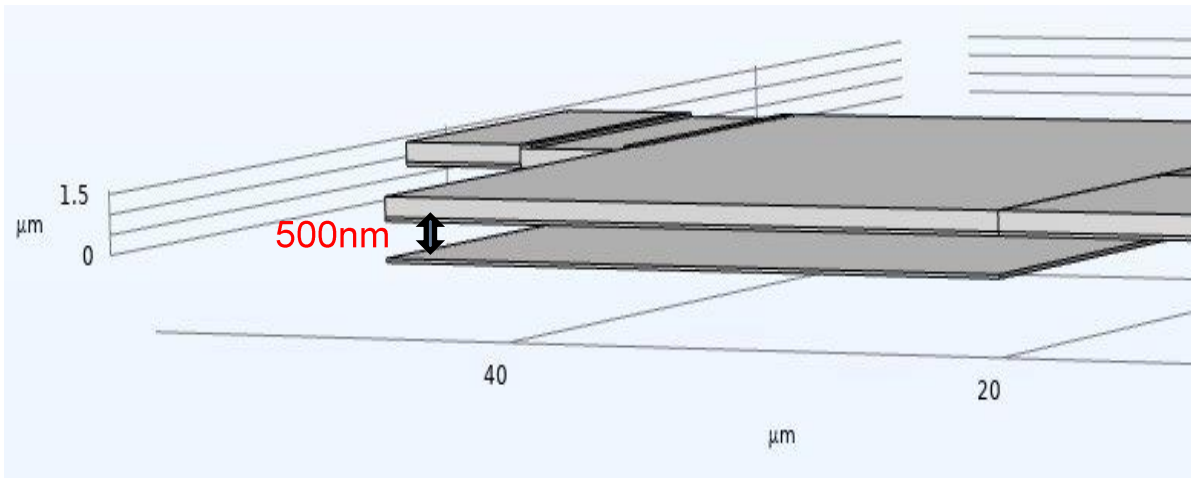
ASU Goals

- Initial design work – proof of concept for working switch structures
- Then, implementation into obfuscation cells and blocks may be initiated



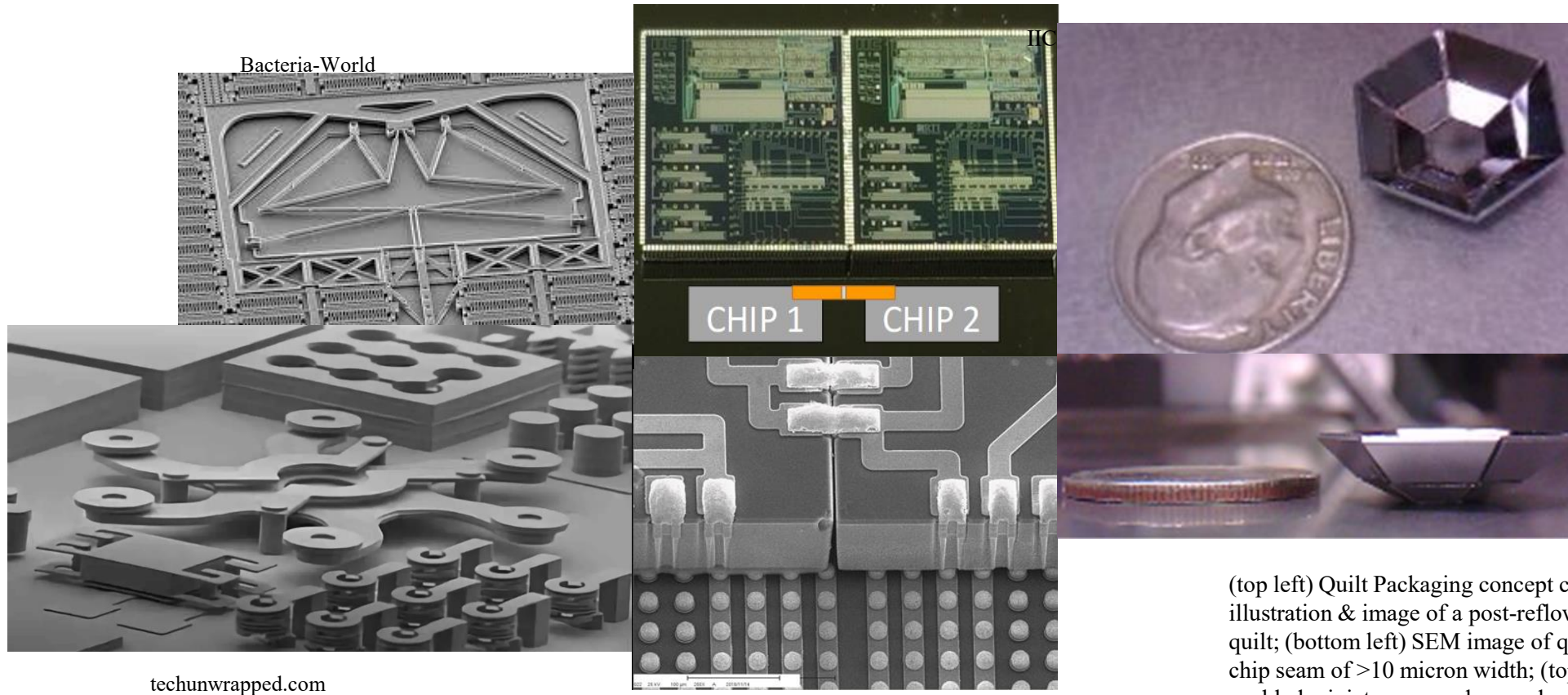
Why MEMS?

- ❑ No leakage current to detect at DC, difficult to detect at AC – Improves security by mitigating successful probing efforts
- ❑ Sub-Micron Air Gap with high aspect ratio to cantilever height – makes optical and electron imaging difficult
- ❑ Large dielectric features relative to metallic features – Further increases electron imaging difficulty
- ❑ Commonly Fabricated – Much industry support from companies like HRL, ADI, TI...etc.



NHanced Semi: Micro-Connections and 3D Structures

MEMS + Precision Electronics



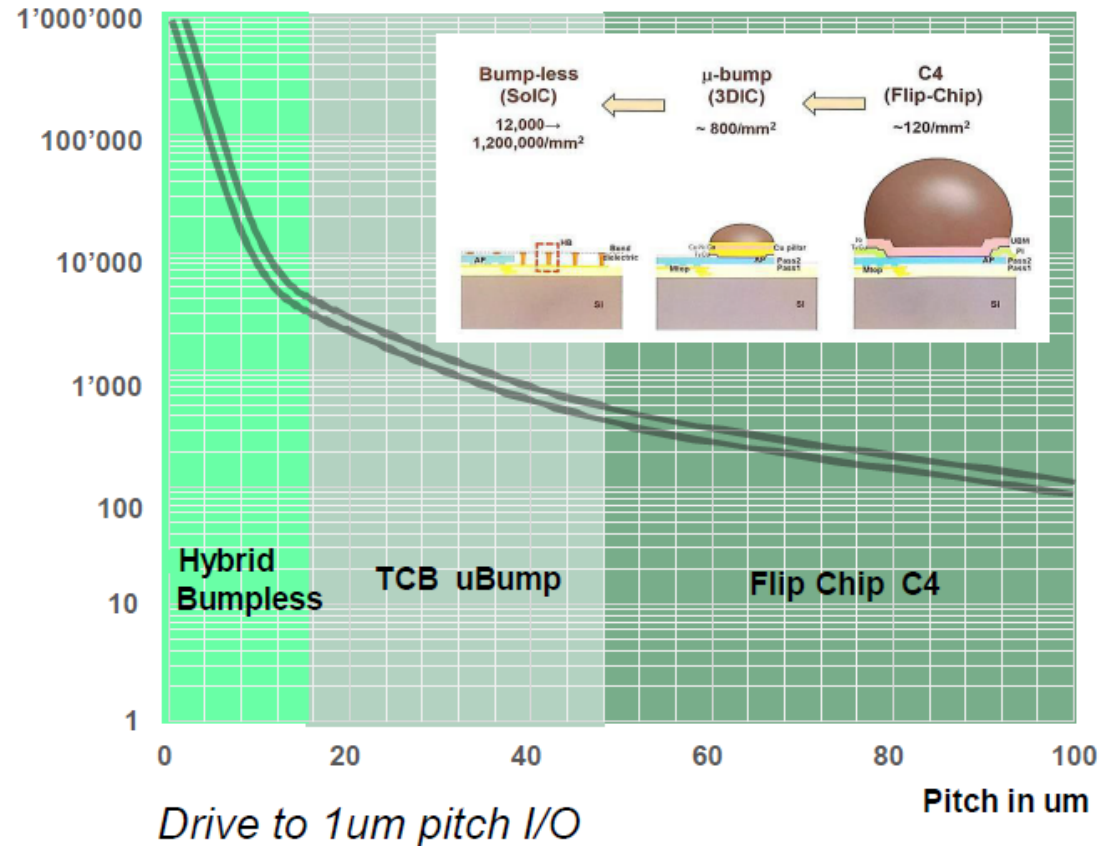
techunwrapped.com

(top left) Quilt Packaging concept cross-section illustration & image of a post-reflowed QP CMOS quilt; (bottom left) SEM image of quilted chip-to-chip seam of >10 micron width; (top right) QP-enabled miniature curved array demonstration article; (bottom right) profile view of QP-enabled miniature curved array.

Hybrid Bonding Innovation

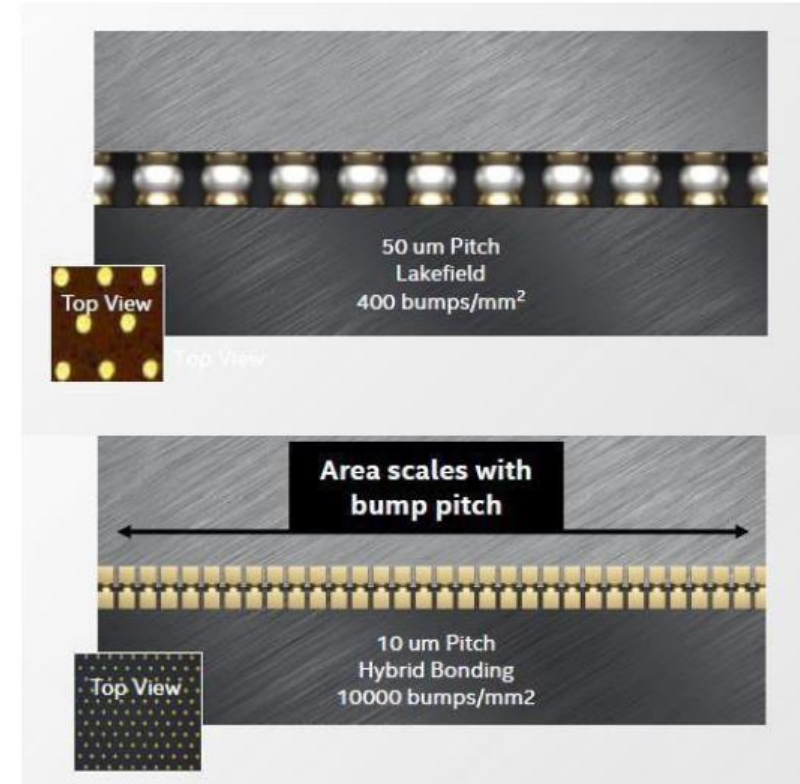
Contacts
Per mm²

Contact Density at Different Contact Pitches



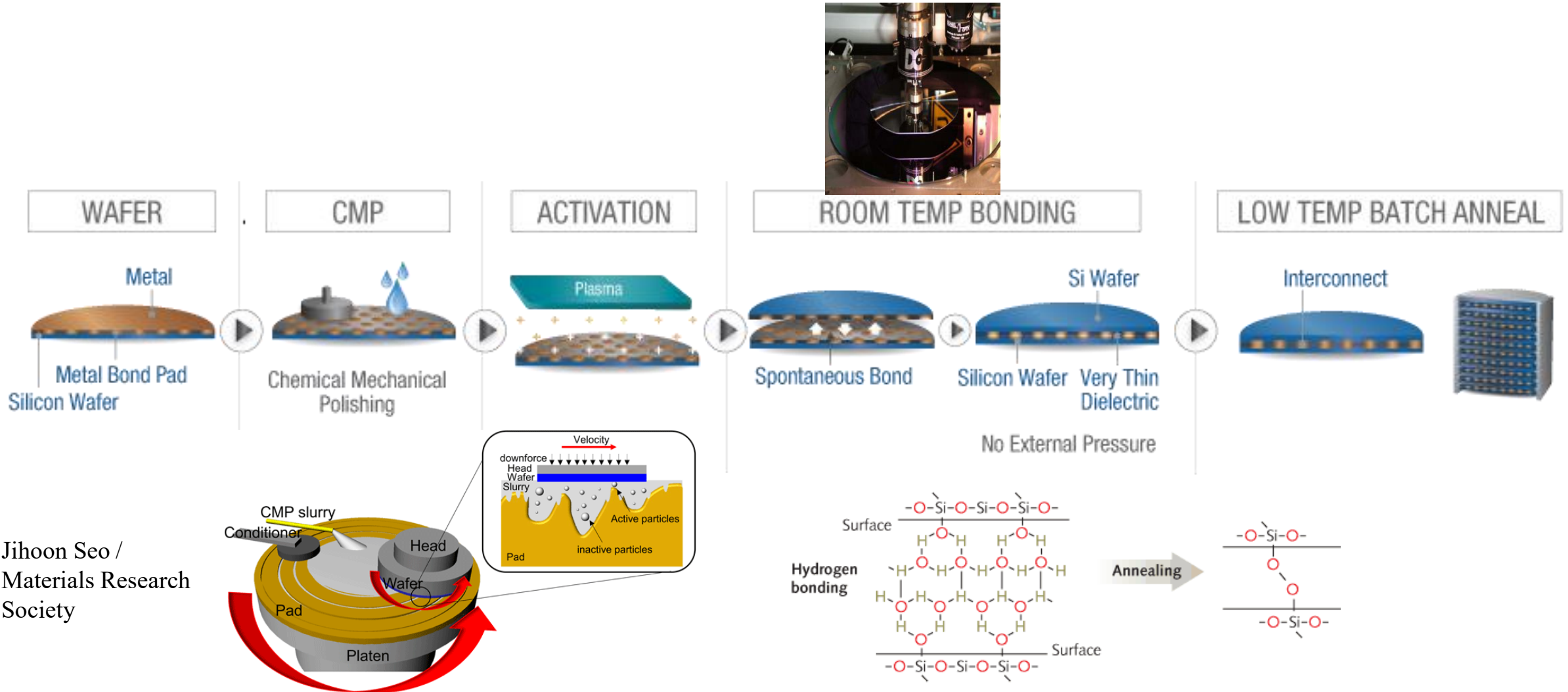
Tom Strothman, BESI

More Contacts Enable More Data

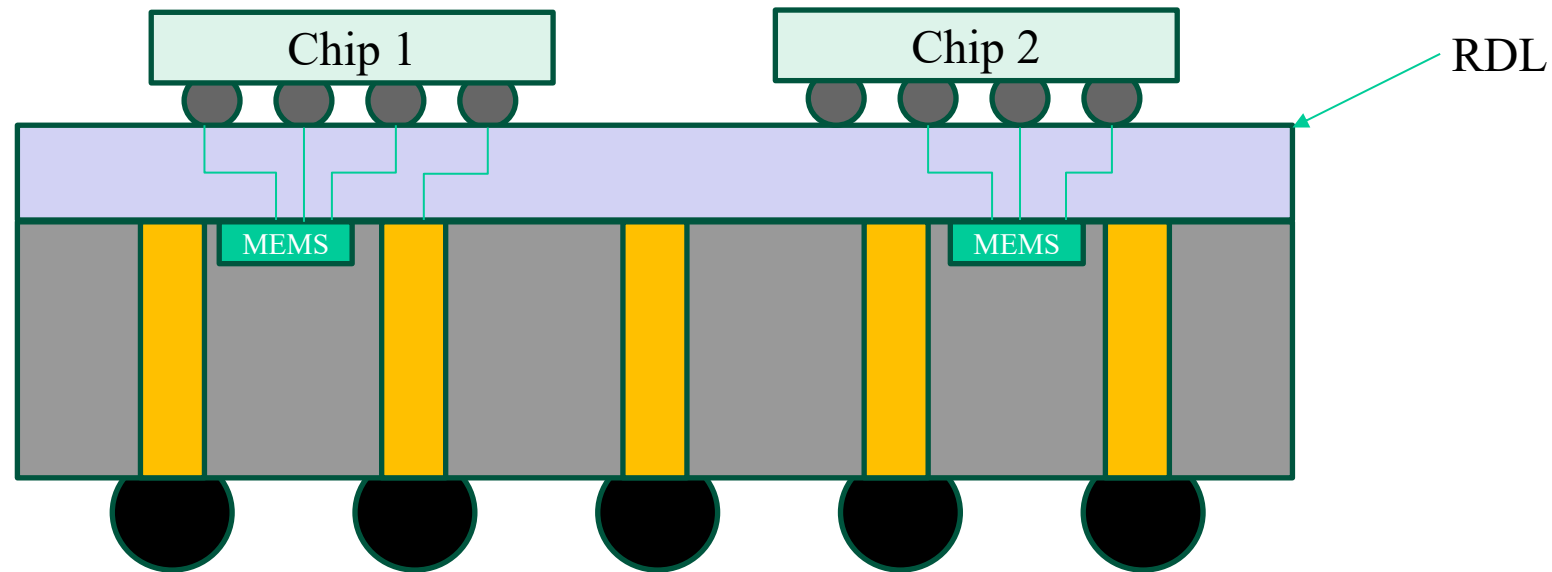


Intel

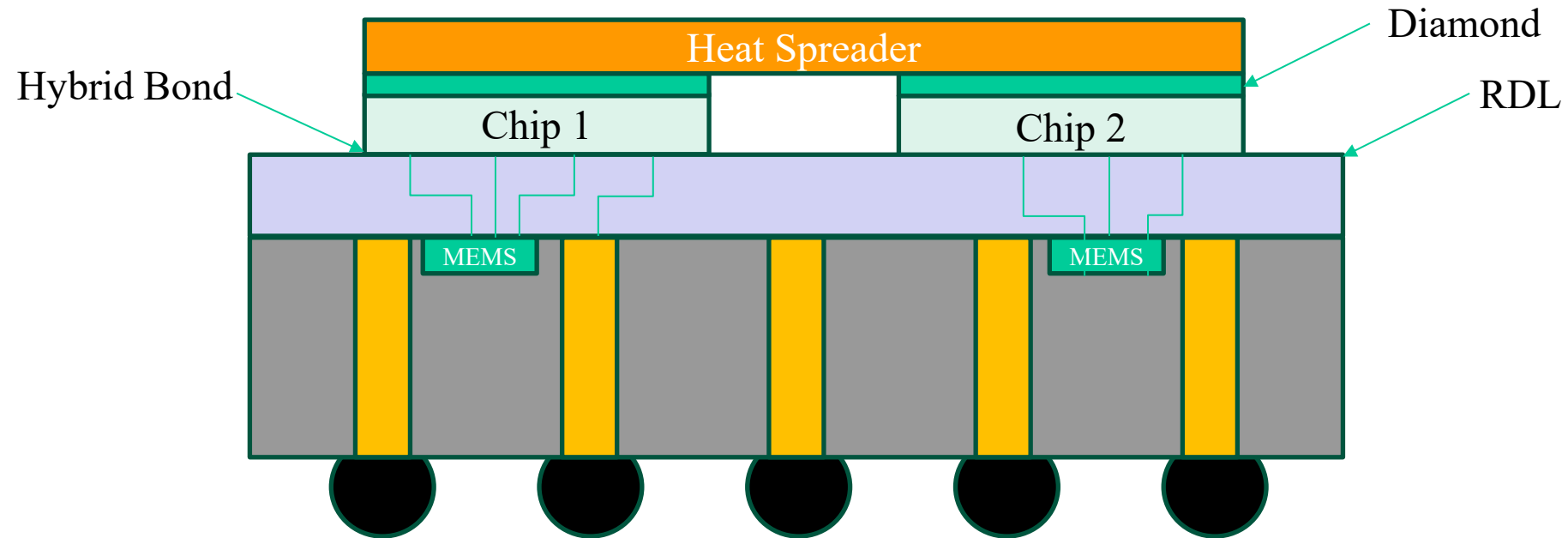
DBI®: Low Temperature Hybrid Bonding Process



Integrate a MEMS Device into a Si-Interposer



High Performance Package Using Si-Interposer



Testing Capabilities at SCAN Lab



Summary

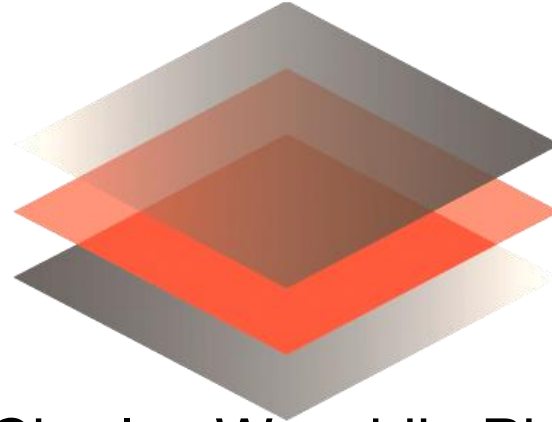
- A new focus on next generation of SECURED PACKAGES
 - Advanced Packaging
 - Unique MEMS arrays prevent replication.
 - Reduced supply chain attack risks.
 - Strong protection against reverse engineering.
 - Future is heterogenous integration using hybrid bonding
 - Interconnect focused – all BEOL additive processing
 - Better ROI
 - Lower development costs
 - Lower CAPEX
 - Leveraging existing foundries
 - Split Fab
 - More Than Moore Technologies
 - IP Centric
 - IP driven value – not cost of capital



Split Rock Lens – StackExchange

System Level Moore's Law

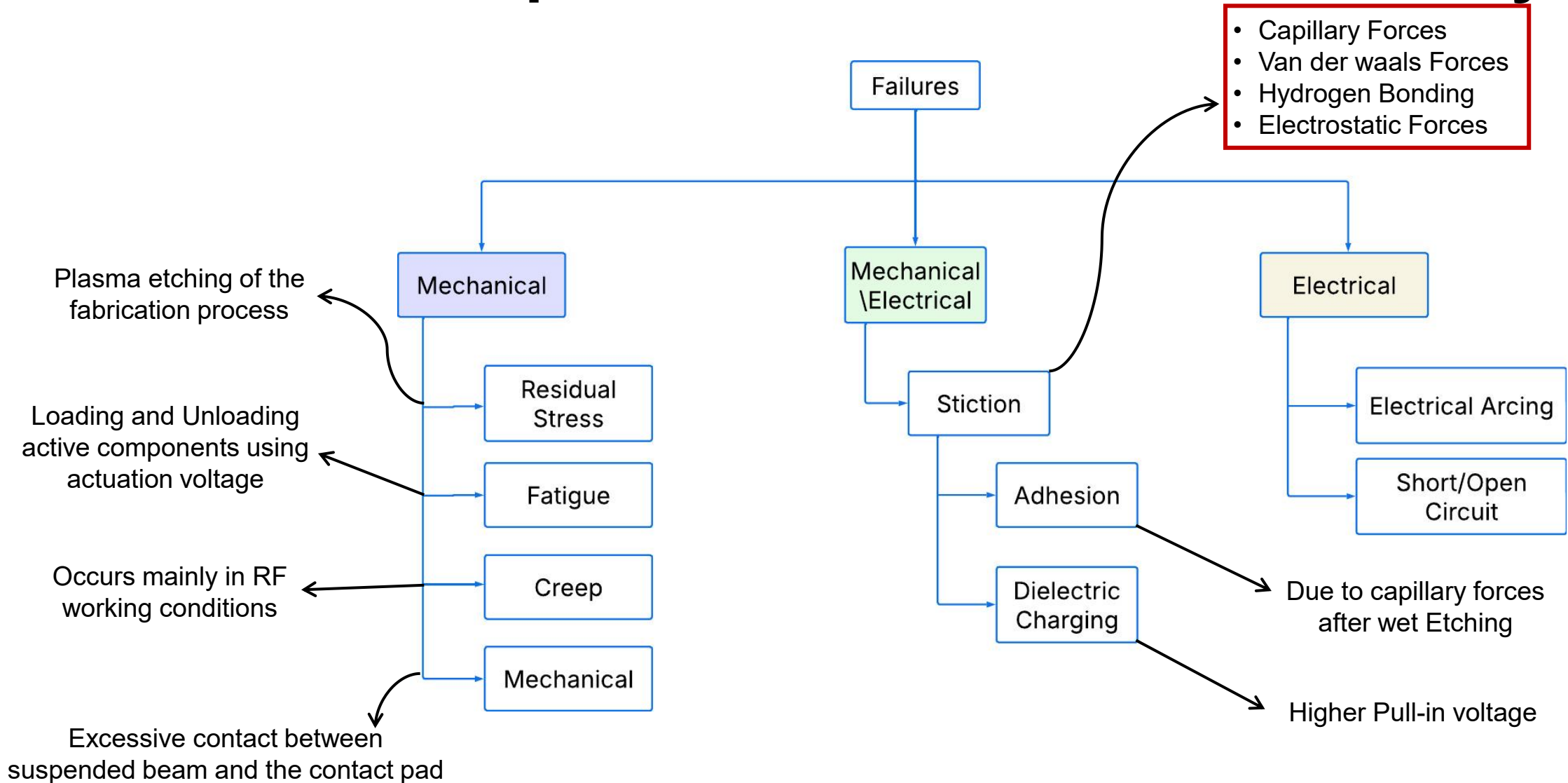
Thank You



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Backup

Failure Map of MEMS Switch for Reliability

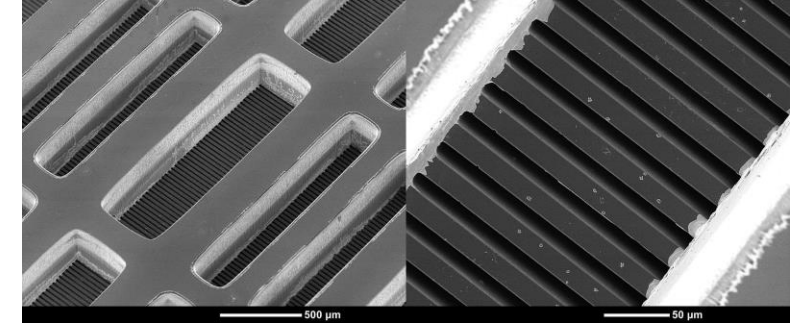


AP Services: Microfluidics and Cooling

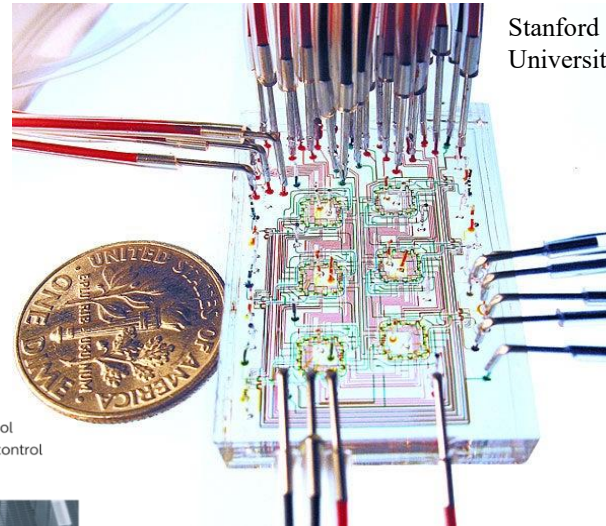
Chip Scale Cooling
For Ultra-Dense Electronics

Biology + Electronics

Purdue

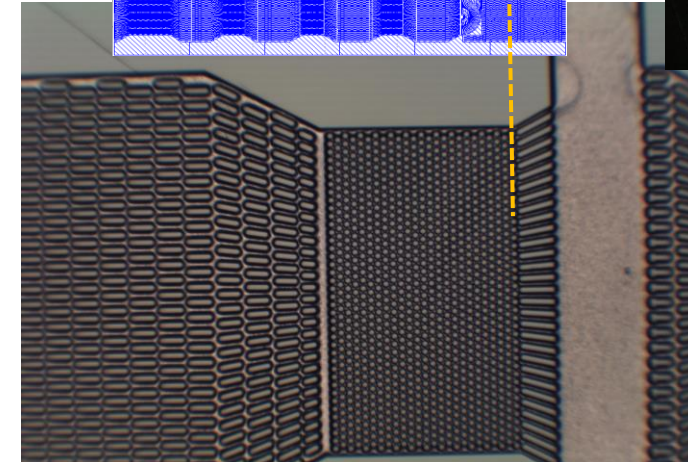
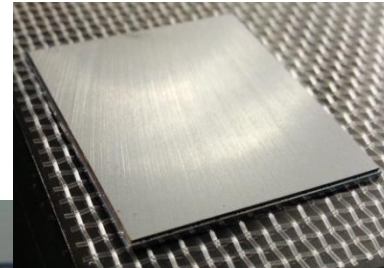
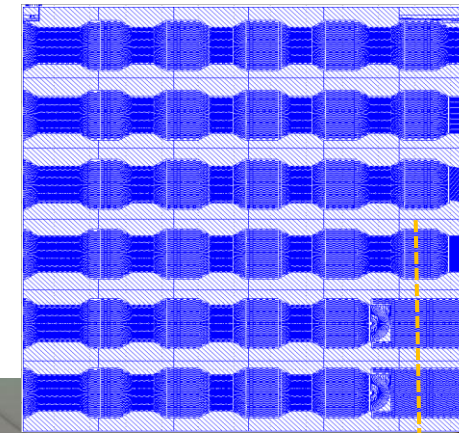
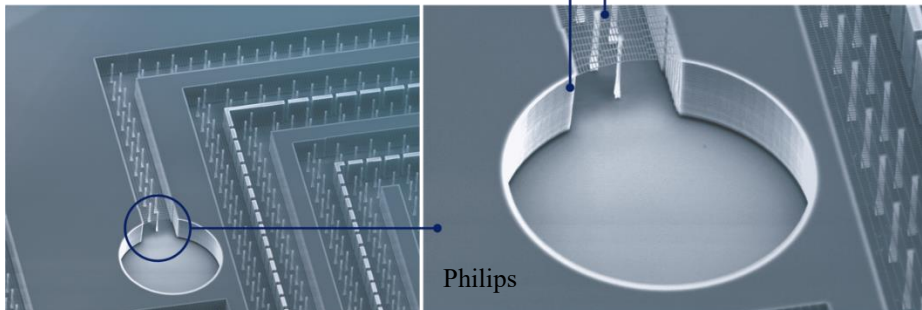


Stanford University



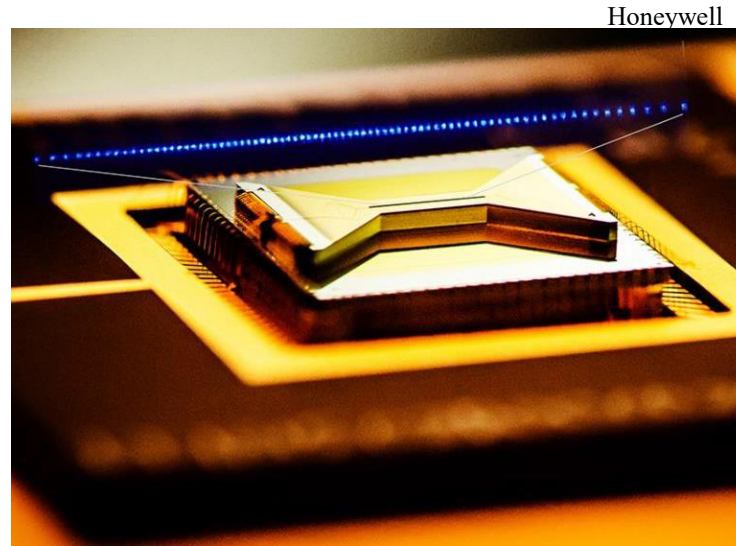
Our state-of-the-art tool set enables us to create microfluidic structures with accurate control:

- <5 degree slope control
- Sub-µm feature size control
- µm range feature size

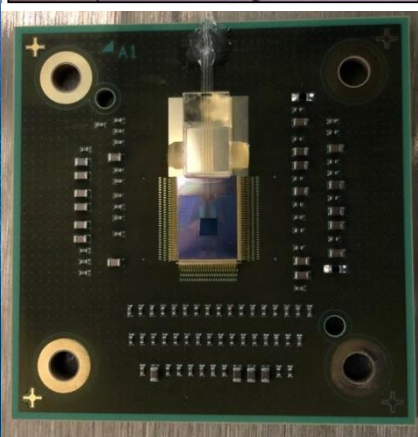
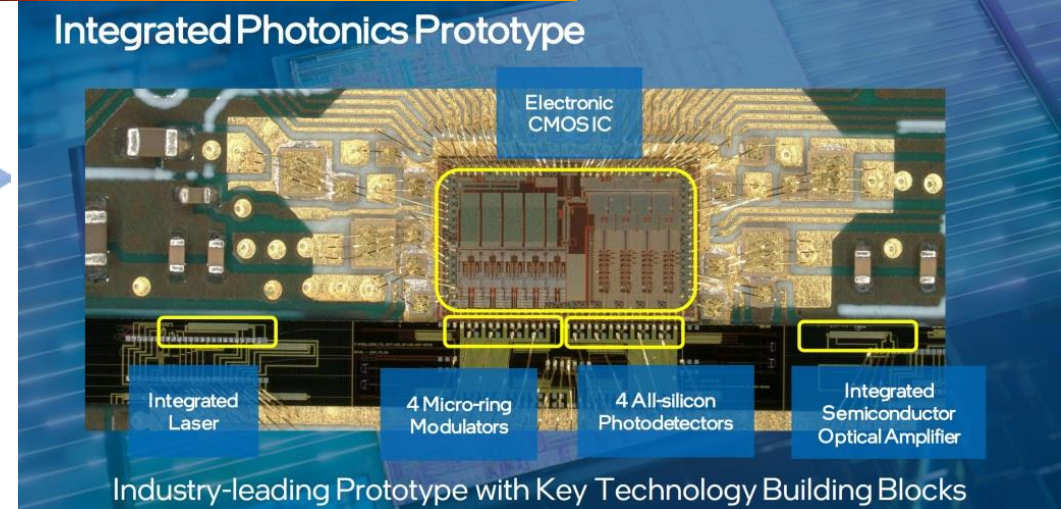
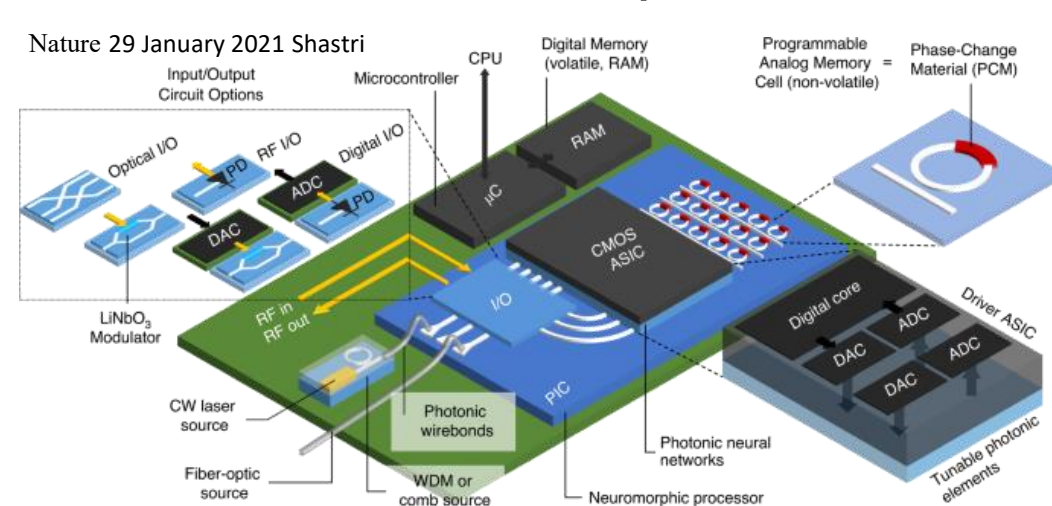
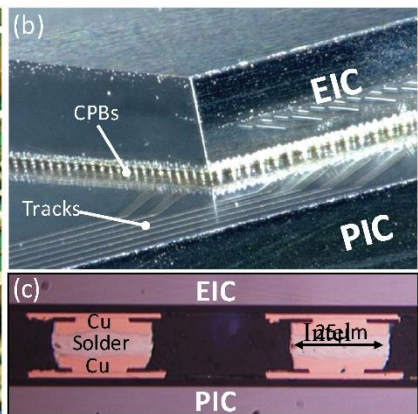
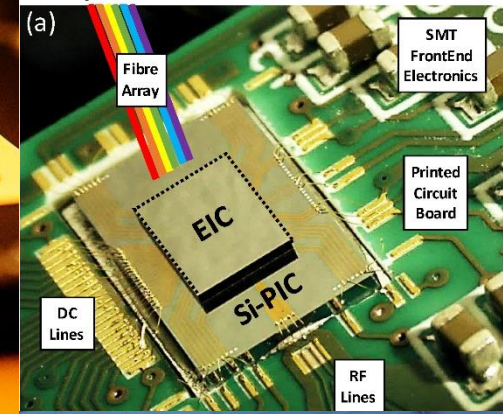


AP Market Drivers: Photonics & Quantum

- I/O
 - Tb/s, $\ll 100\text{fJ/b}$
 - SiP 500ff I/O Load
 - 2.5D 25ff I/O Load
 - 3D 3ff I/O Load
- Processing
 - “Quantum Leaps”



Tyndall National Institute Carroll et al



AP Market Drivers: Intelligent Sensors and Edge Compute

- Communication is limited
 - Data movement costs power
 - Data movement costs time
 - Data movement costs money
 - You can't always “phone-home”

