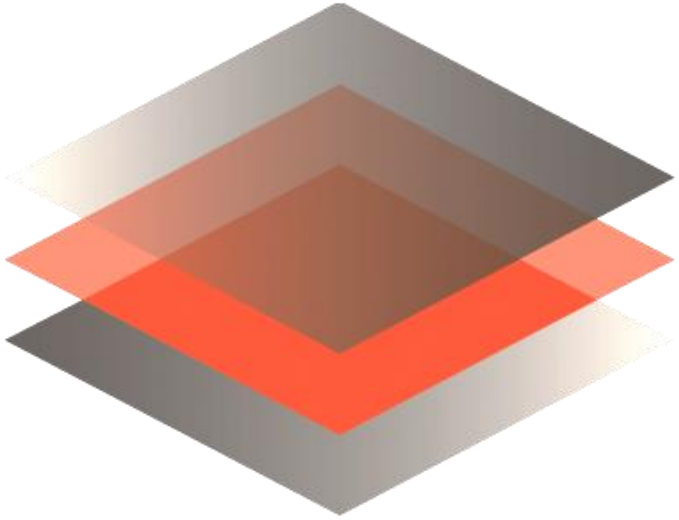
29th Lithography Workshop



June 2026

Robert Patti

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630-561-6813

NHanced SEMICONDUCTORS

Our Story & Recognition

- Founded in 2016 with a seasoned core team
- U.S. Owned & Headquartered in Batavia, IL
- AP Technology Leadership in Hybrid Bonding Processes
- Extensive Experience with 2.5D & 3D Heterogeneous Integration
- 100+ Employees with Industry Recognized AP Experts on Staff

Fermilab

Recognized for our role in the building of 2.5D Interposer Assemblies

L3HARRIS™

"Small Business Supplier of the Year"

Forbes

Article: "Compute Cambrian Explosion"

2022 3DInCites AWARDS WINNER

"Engineer of the Year"
Dr. Sangki Hong

Microwave Journal
Frequency Matters.

"Fabs and Labs Department"

2025 3DInCites AWARDS WINNER

3D Hybrid Integration
(one of five awarded for Technology Enablement)

ElectronicDesign

NHanced SEMICONDUCTORS

Quantum Computing Inc. Completes Acquisition of NHanced Semiconductors, Inc.

Strategic acquisition launches Fab 2 to accelerate key roadmap initiatives and expands manufacturing capabilities

HOBOKEN, NJ – JUNE 23, 2026 –Quantum Computing Inc. (“QCi” or the “Company”) (Nasdaq: QUBT), an innovative, quantum optics and integrated photonics technology company, today announced the completion of acquiring NHanced Semiconductors, Inc. (“NHanced”), for a combination of cash and QCi stock valued at $73.1 million, subject to customary adjustments, and up to an additional $72.0 million if certain performance targets are achieved (the “Transaction”).

The acquisition marks an important step in QCi’s transition from research-driven innovation and prototyping to scalable commercial production. By adding semiconductor and nanophotonics fabrication capabilities, advanced packaging expertise and specialized engineering talent, QCi is strengthening its operational capabilities and manufacturing readiness. Advanced photonics technology and manufacturing are at the core of QCi’s commercialization roadmap. The recent acquisition and successful integration of Luminar Semiconductor Inc. have installed world-class expertise and fabrication in laser, light detection, photonic packaging, and testing at QCi. This acquisition will provide the foundation for scalable chip-manufacturing of the Company’s quantum and photonics technologies, supporting commercialization efforts and advancing its vision of a vertically integrated platform spanning research, development and manufacturing. It positions QCi to address growing market demand across quantum computing, sensing, networking, and photonics markets while accelerating the path from innovation to market deployment. Aside from its quantum technology and product portfolio, QCi now also offers leading-edge services, products, and solutions in semiconductor and nanophotonics manufacturing, lasers, detectors, testing, and packaging.

…

NHanced SEMICONDUCTORS

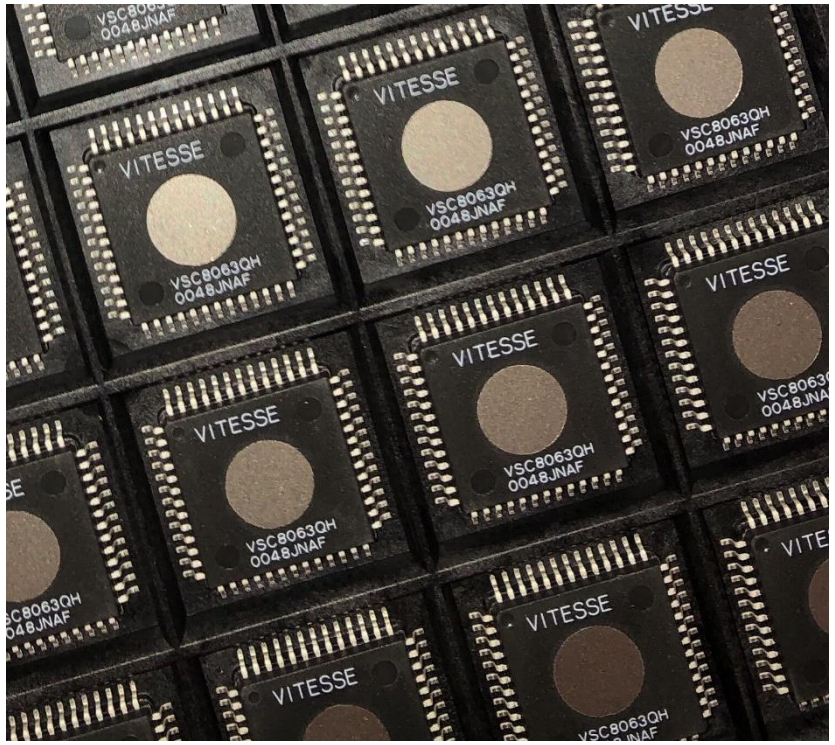
How It Started for NHanced…

1988
2,000 gate equivalents
325MHz FF Toggle Rate
~2M Transistors
1.2um 2 metal CMOS Process

This is a great part, but can we make it better…

We Are Going to Build a 0.8um GaAs 3020!

- GaAs is the material of the future!!
  - Higher performance with CMOS like processing
    - Lower voltage
    - Scalable
    - Good yields
    - FF Toggle Rate >2GHz
      - 10x CMOS at the same node



But…

It failed to out-perform CMOS…

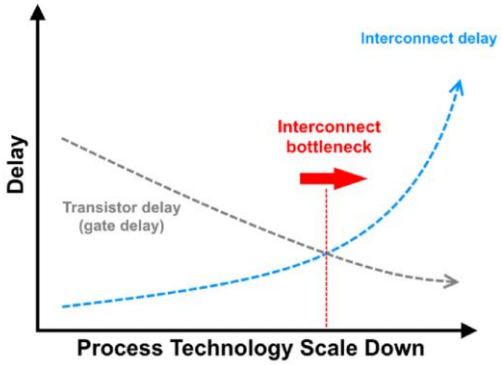
The next gen CMOS Xilinx 4000 Series came out and it ran faster even though the FF toggle rate was only ~30% of the GaAs.

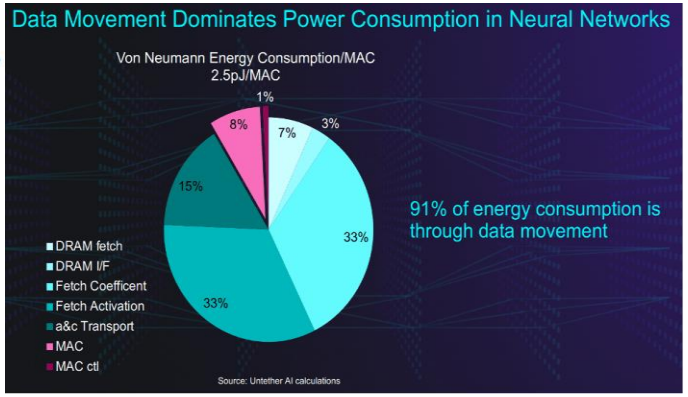
Why?

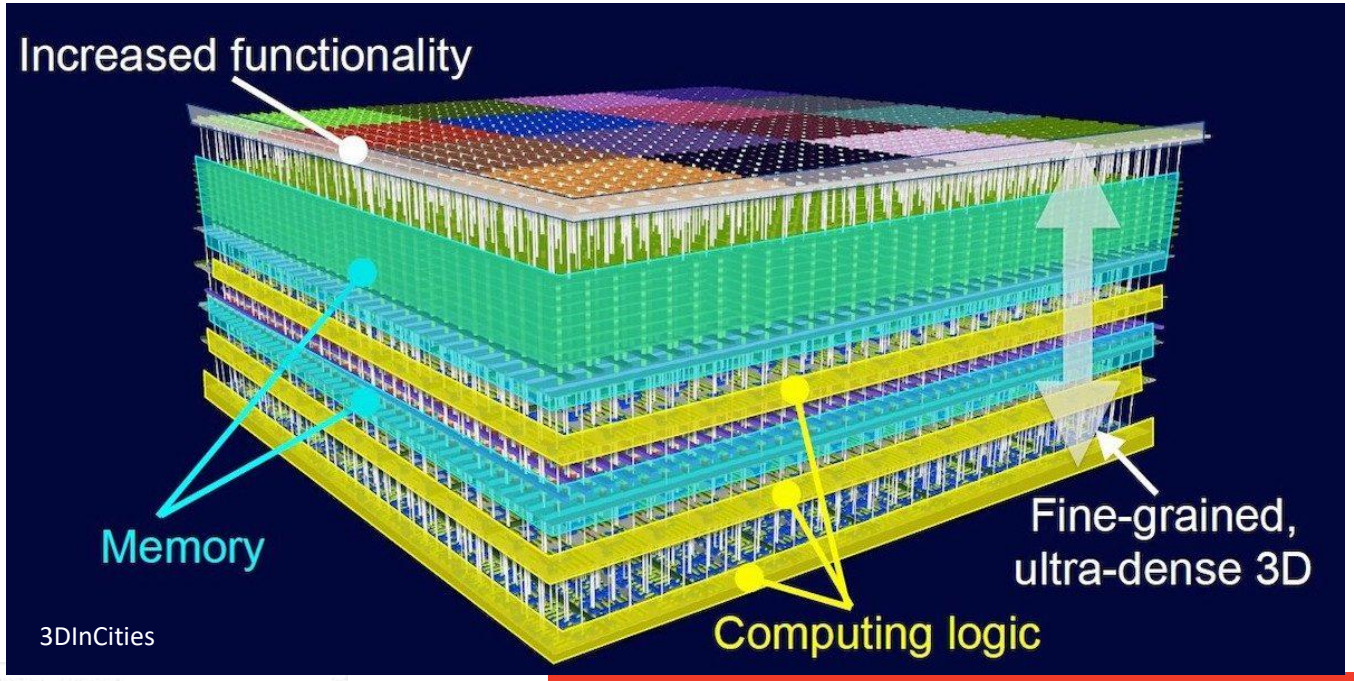
It's All About The Wire

- Wire length controls the delay
  - Span of control
- Accounts for majority of power usage
  - Memory fetch is an extreme example

By the mid 90's wire was already becoming the dominant delay limiting performance. The GaAs FPGA demonstrated this perfectly. The transistor performance improvement of GaAs didn't matter for the FPGA. ***It was the wire.***







NHanced SEMICONDUCTORS

Foundry 1.0: The Industry Today

- Current semiconductor business has been focused on driving smaller transistors.
- This is a safe path with 50 years of historic success!
- But…
  - High development cost
  - High capital cost
  - Long development times
  - Expensive design tools
  - High risk
- It is the Twilight of Moore's Law


TSMC

Effective End of Moore's Law

Moore's Law was first and foremost a statement about economics. We could shrink transistors and build more of them for about the same cost.

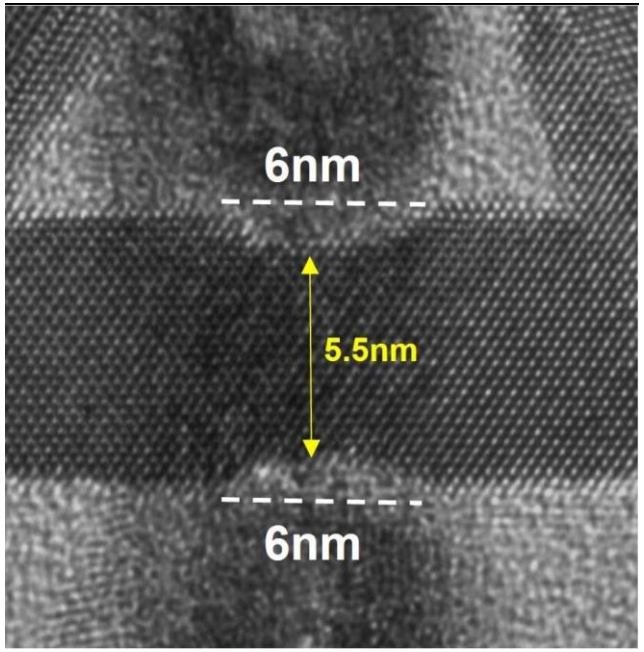
- This has been the basic premise of the semiconductor industry for 50 years and was true up until the last few years.
- Today we can indeed shrink transistors further, but the cost per transistor no longer declines.

  We can get something a little more compact

  - Perhaps a little less power
  - But we pay more for these features now.

2^{20} Scaling in 40 years
$2\mu m \rightarrow 2nm$

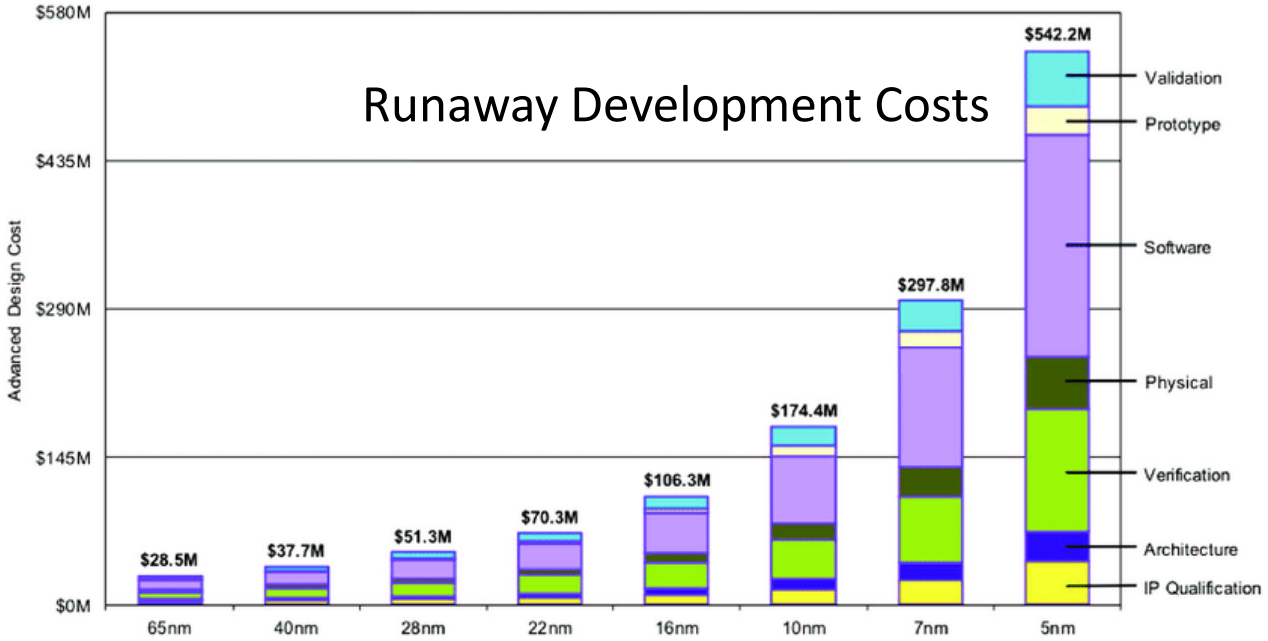
Intel



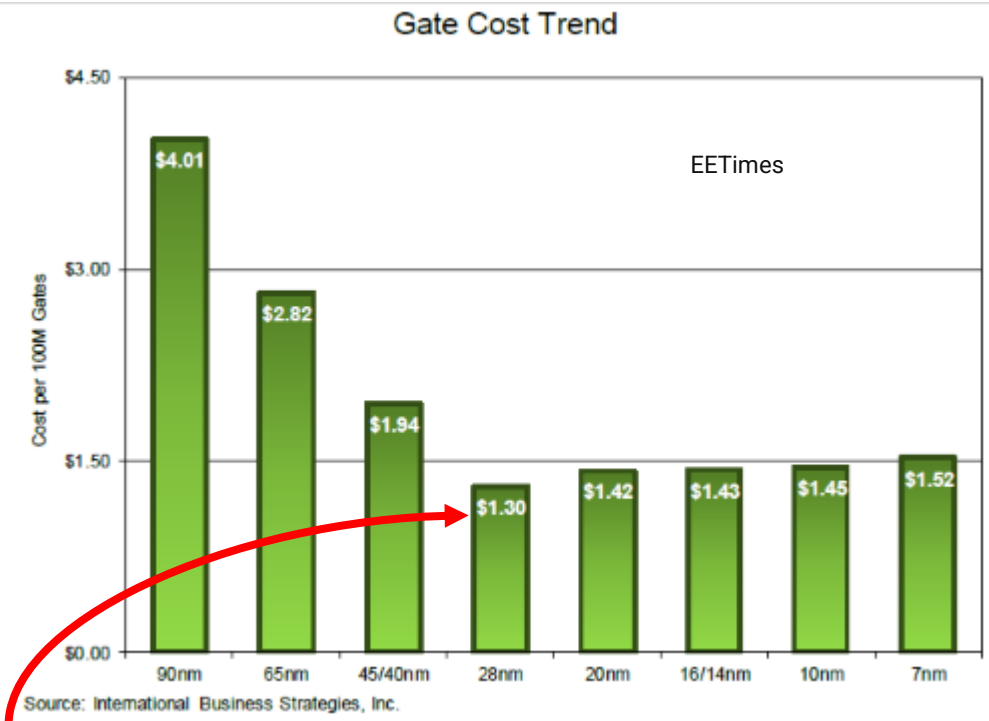
One can see the atoms with this 6nm device. It is obvious we can't scale much more.
Maybe to 1nm?

NHanced SEMICONDUCTORS

Moore's Law Is About Cost

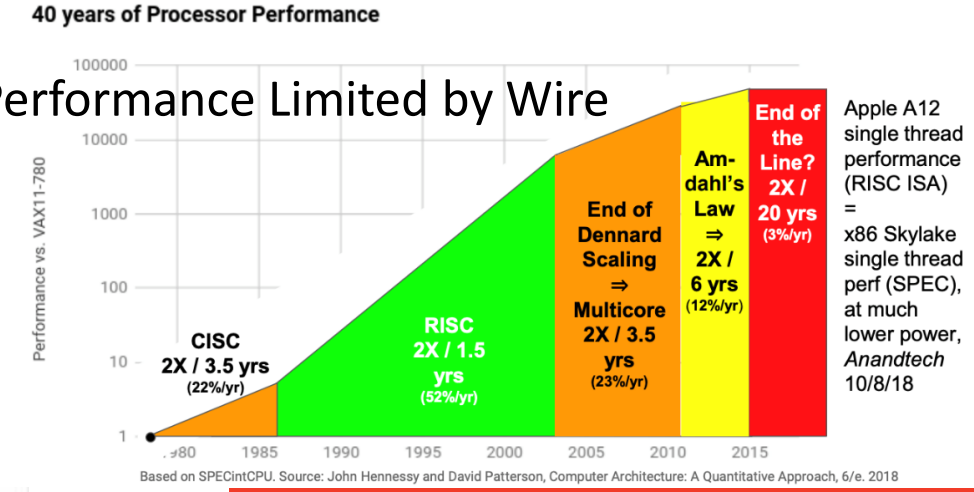


Chip Design and Manufacturing Cost under Different Process Nodes: Data Source from IBS



End of Growth of Single Program Speed?

Single pattern 193i lithography reaches its limit. Smaller nodes required double patterning and/or EUV. Lithography already the single most expensive step in semiconductor manufacturing doubles or triples in cost after the 28nm node – effectively ending Moore's Law.



Apple A12 single thread performance (RISC ISA) = x86 Skylake single thread perf (SPEC), at much lower power, *Anandtech* 10/8/18

NHanced SEMICONDUCTORS

What Does This Mean?

The semiconductor industry is about to undergo a sea change.

- New ways of accomplishing Moore's law economics and performance are needed.
  - The industry is now looking to use advanced packaging to drive future semiconductors.
    - Better Cost
    - Better Performance
    - Better SWaP

The revolution in semiconductors is reminiscent of the revolution in locomotives. The locomotive builders reached a tipping point driven by cost. After which, diesels which had been around for 20 years, almost over night replaced steam locomotives. The steam engine incremental improvements no longer were ample to sustain the industry.

The economics drove the change.

A New Semiconductor Industry Paradigm

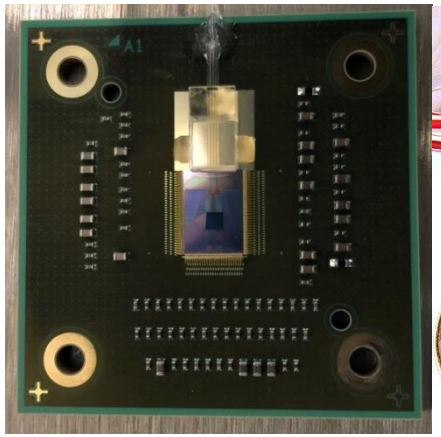
Foundry 2.0 –

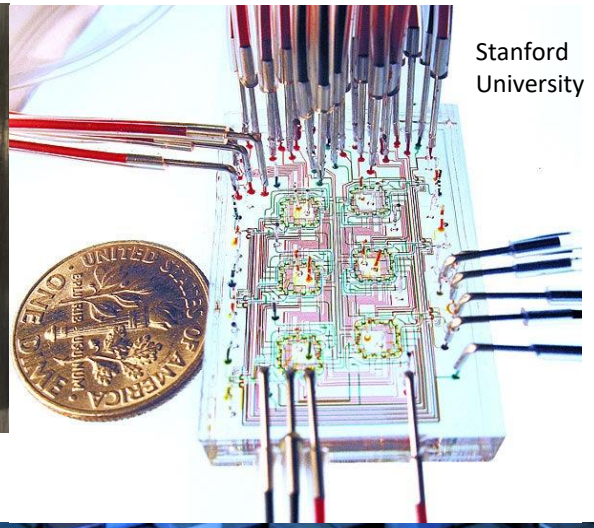
A Finishing Foundry that takes the standardized building blocks from traditional semiconductor manufacturers and uses advanced packaging and additive manufacturing to create highly customized components with superior performance targeting small and medium sized markets.

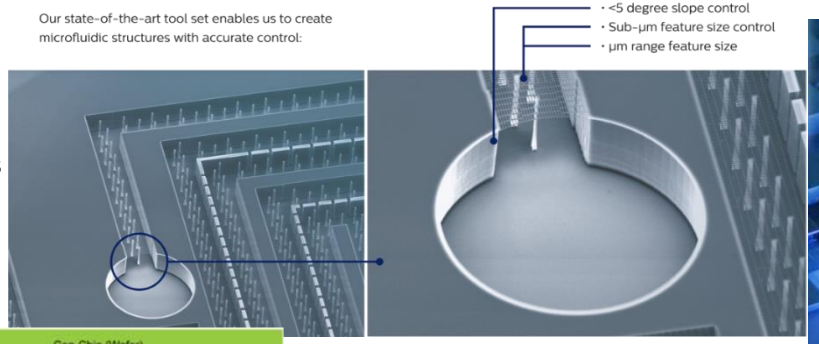
NHanced SEMICONDUCTORS

Foundry 2.0

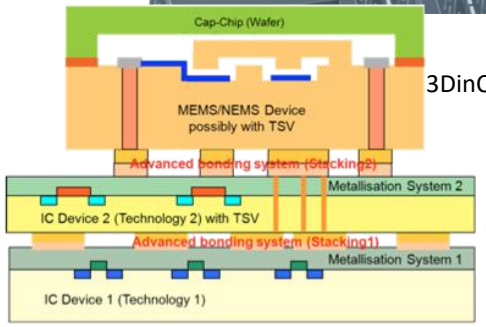
- System solution focus
  - Best of class components
- Relies on Advanced Packaging (AP) and Chiplets
  - Heterogenous integration
  - Photonics
  - MEMS
  - RF
- Advantages
  - Low development cost
  - Low capital cost
  - Short development times
  - Inexpensive design tools
  - Low risk



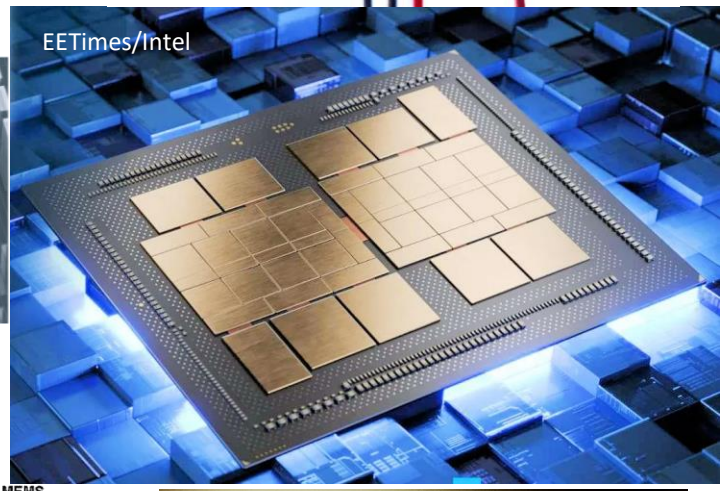


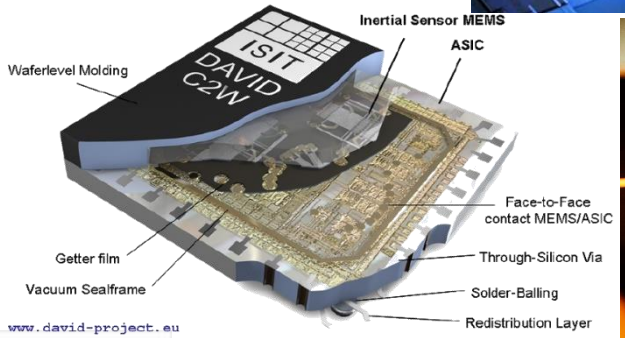


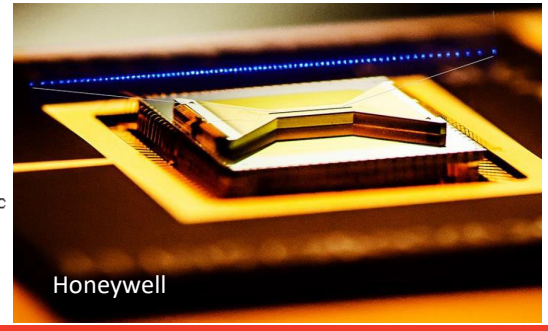
Philips



3DinCites





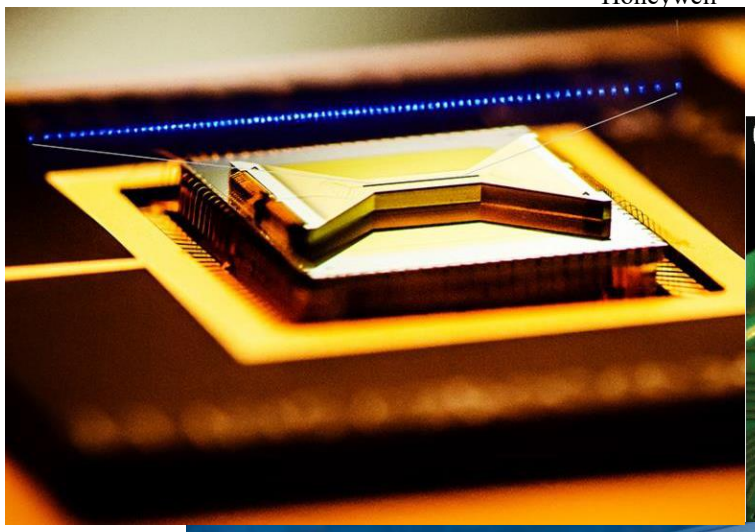


NHanced SEMICONDUCTORS

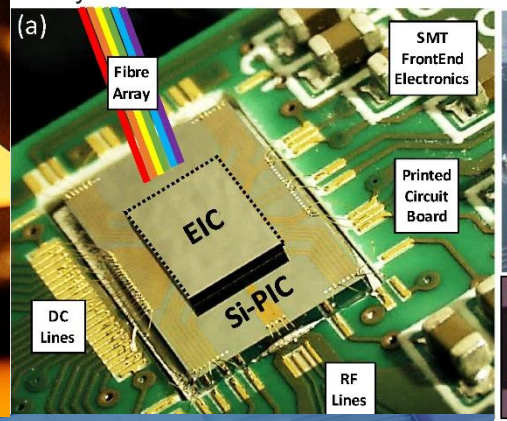
AP Drivers: AI, Quantum, & Integrated Sensors

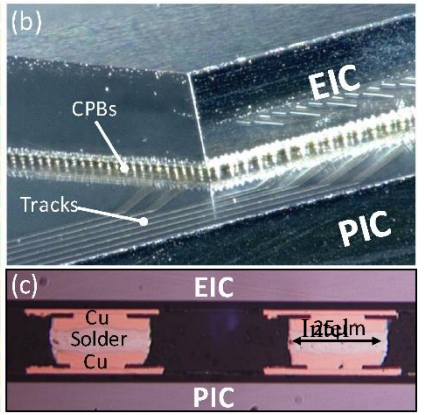
- Advanced Packaging I/O
  - Tb/s, <<100fJ/b
    - SiP 500ff I/O Load
    - 2.5D 25ff I/O Load
    - 3D 3ff I/O Load
- AI Musts:
  - Local Memory
  - >100TB/s

Honeywell

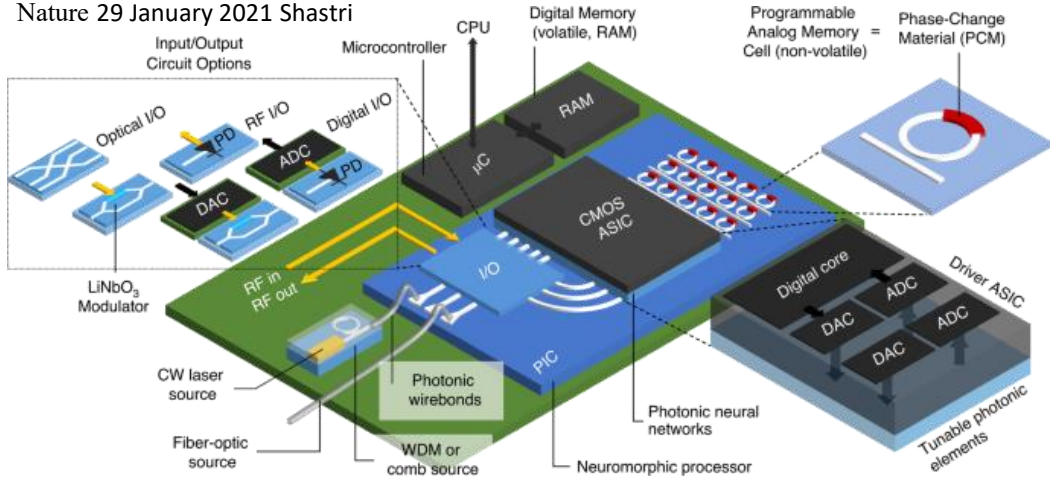


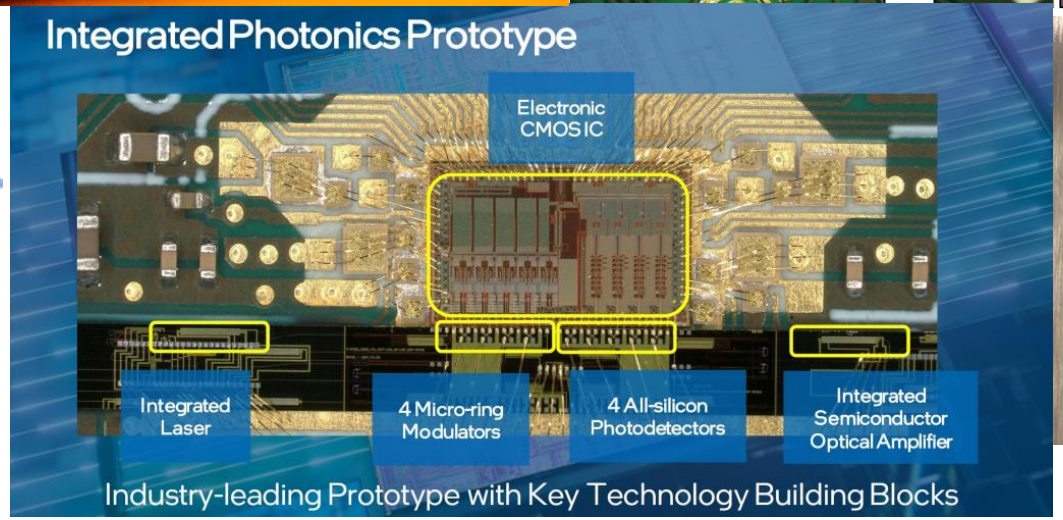
Tyndall National Institute Carroll et al

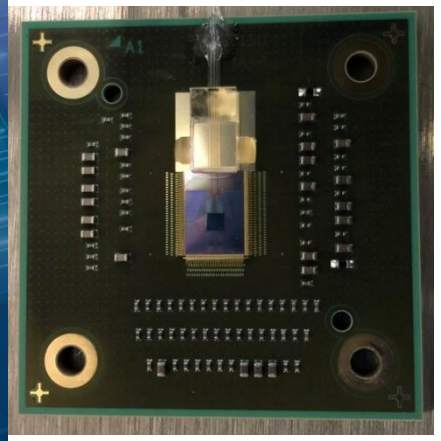




Nature 29 January 2021 Shastri







NHanced SEMICONDUCTORS

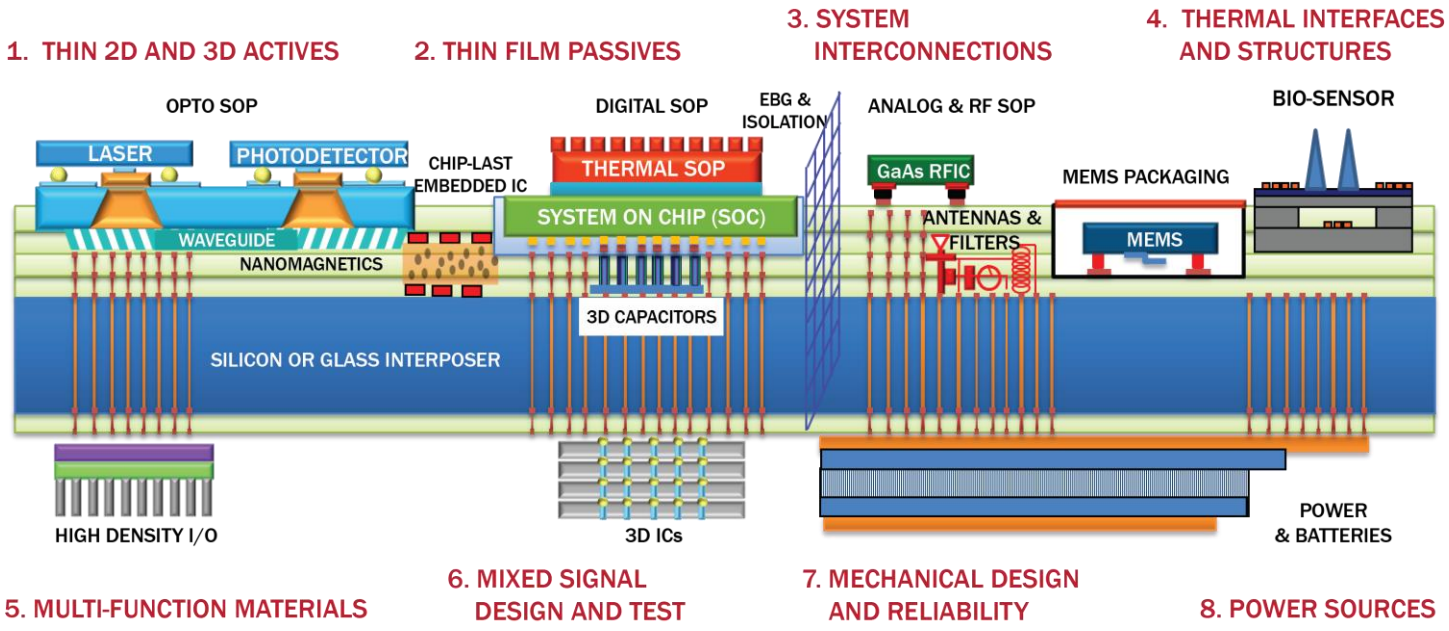
AP Drivers: Internet Of Things

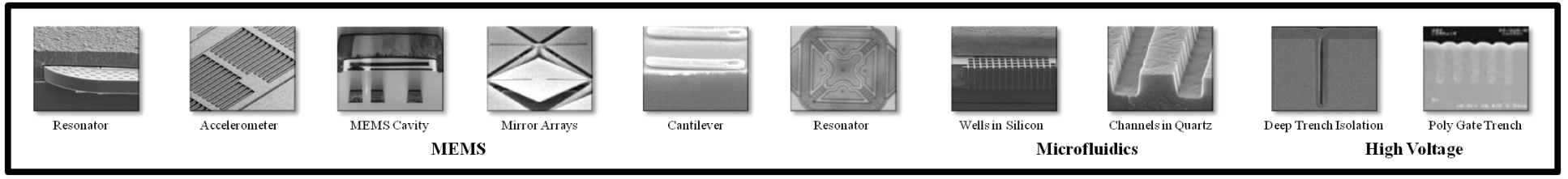
The IoT requires sensors, processors, RF, energy harvesting, and often special materials to meet the industry needs.

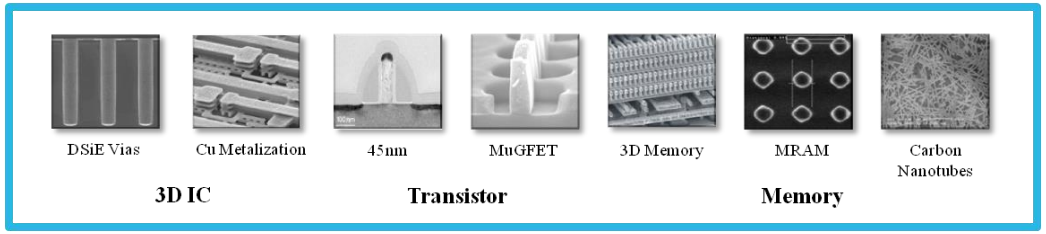
More Than Moore

GEORGIA TECH PRC

These new technologies and IoT are requiring introduction of new materials and processes that are often incompatible with CMOS. Advanced Packaging provides a mechanism for the tightly coupled integration of these new elements into true complete systems in a package with often far superior performance and lower power.







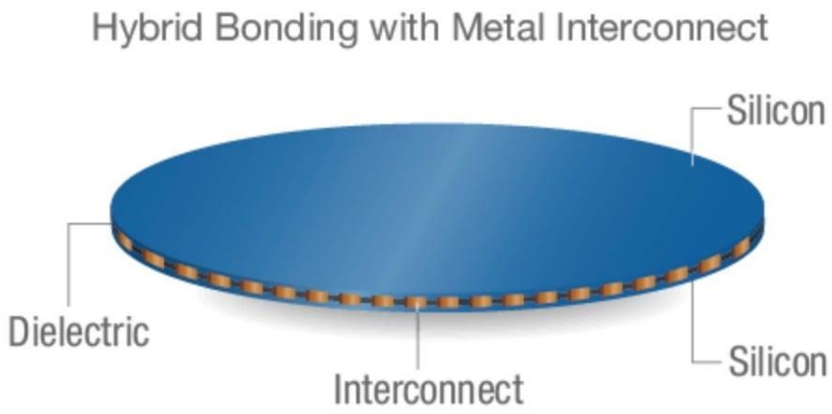
NHanced SEMICONDUCTORS

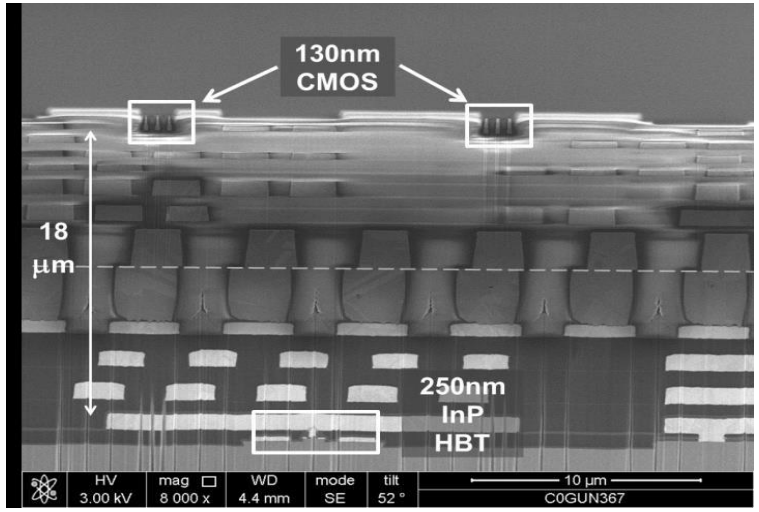
Hybrid Bonding – A Keystone Technology

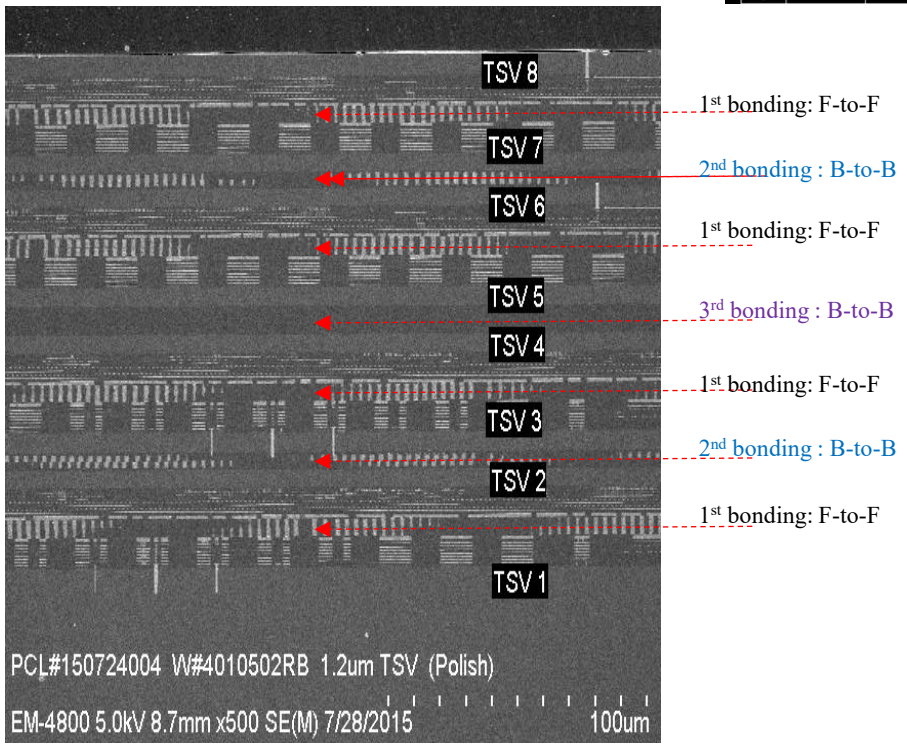
The **Enabler** for Next Generation Advanced Packaging.

DBI® Advantages

- Higher Bandwidth
- Reduced Latency
- Increased Efficiency
- Higher I/O Density
- Scalable (<1µm Pitch)
- Low Temperature Bonding







1st bonding: F-to-F

2nd bonding : B-to-B

1st bonding: F-to-F

3rd bonding : B-to-B

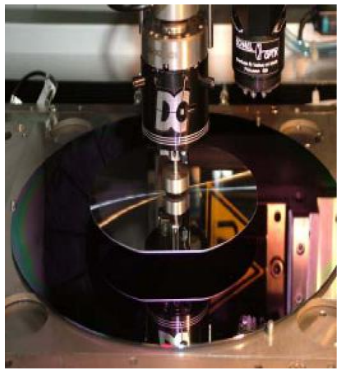
1st bonding: F-to-F

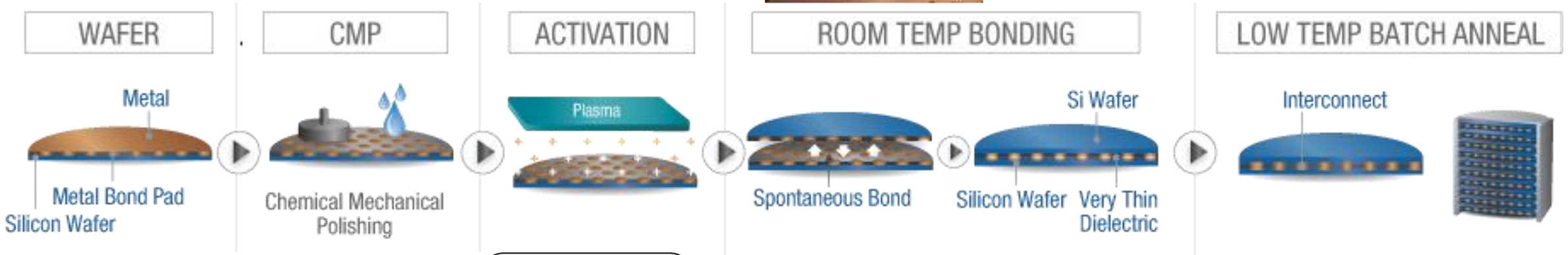
2nd bonding : B-to-B

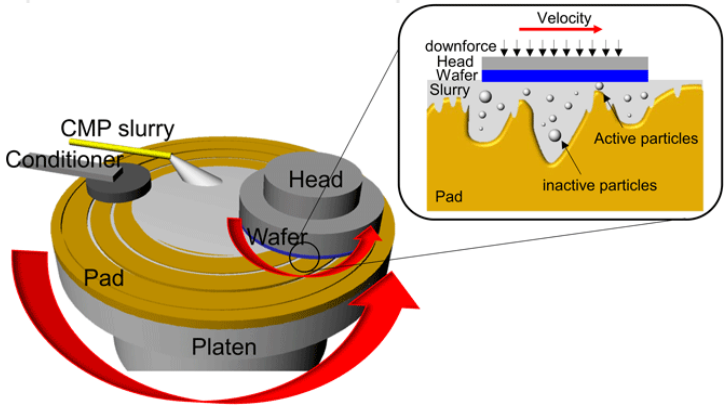
1st bonding: F-to-F

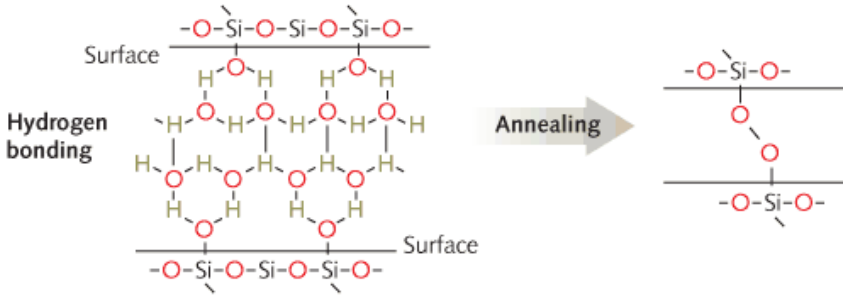
NHanced SEMICONDUCTORS

DBI®: Low Temperature Hybrid Bonding Process





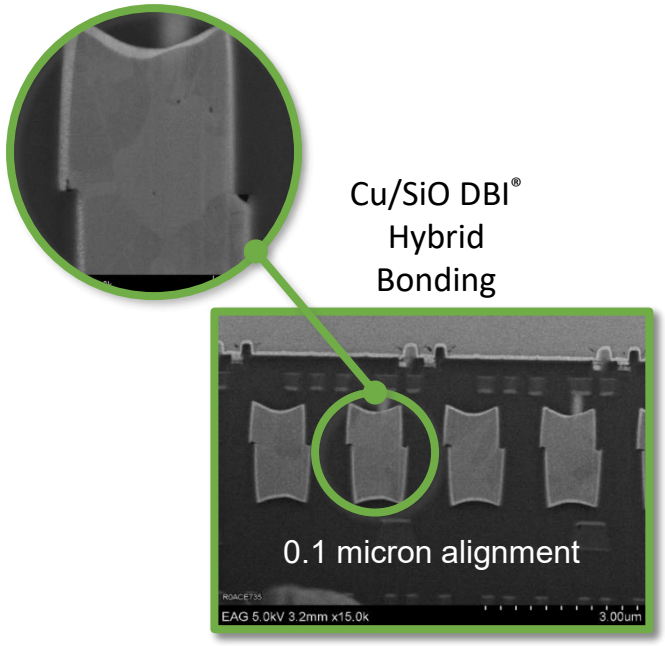




Jihoon Seo / Materials Research Society

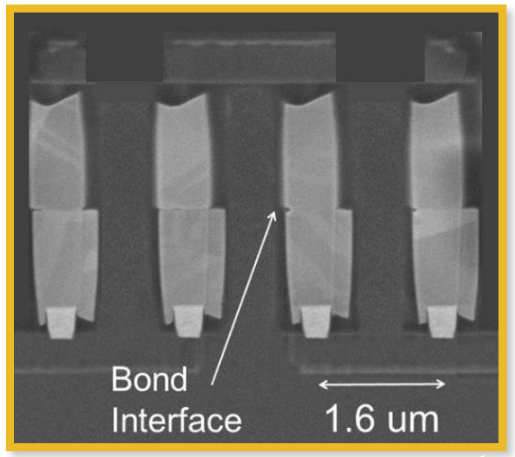
NHanced SEMICONDUCTORS

Hybrid Bonding Interconnect Pitch Scaling

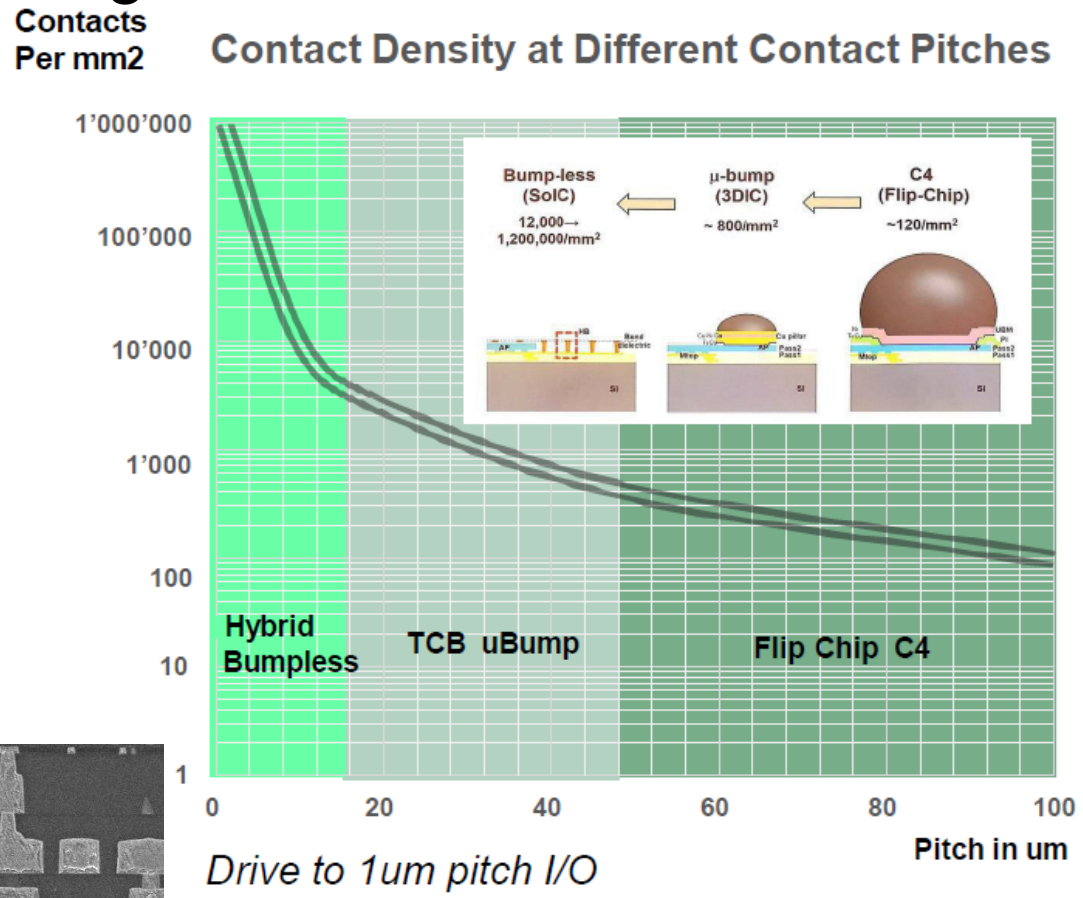


1.9 µm DBI® pitch, 300℃

Scalable To < 1um Pitch
0.8um Pitch Demonstrated

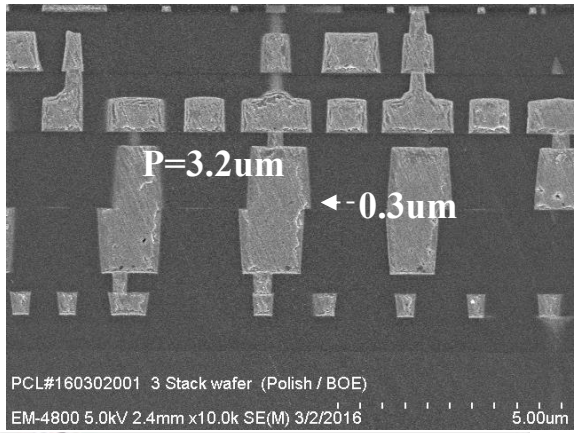


1.6 µm DBI® pitch, 300℃



Drive to 1um pitch I/O

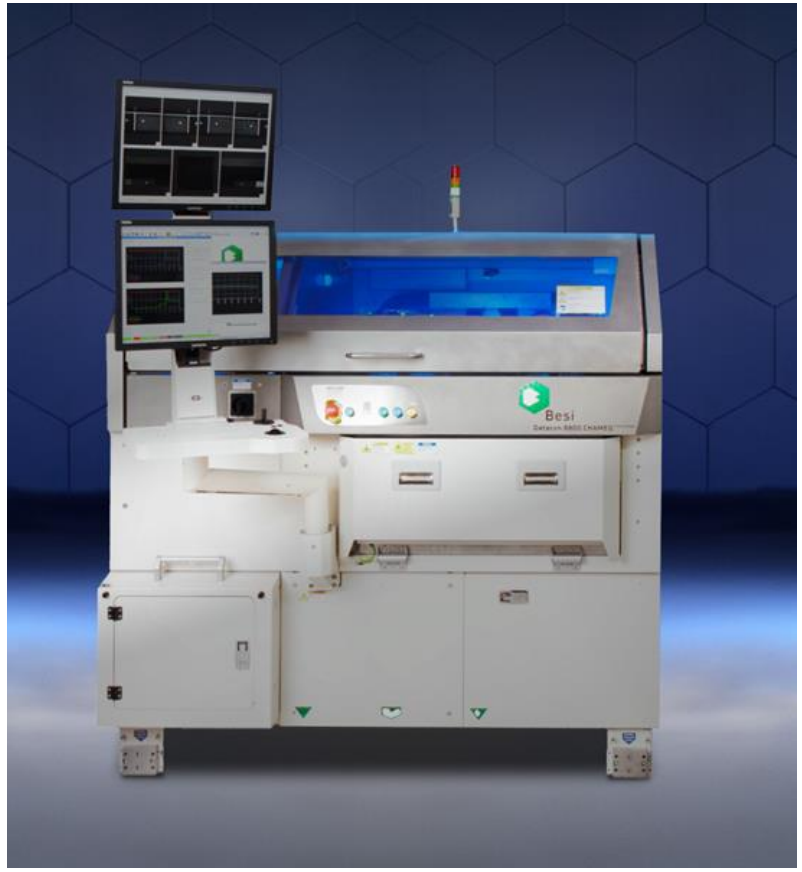
- WtoW 3sigma < ±1um misalign performance
- DtoW 3sigma < ±100nm misalign performance
- Production Minimum pitch = 2um



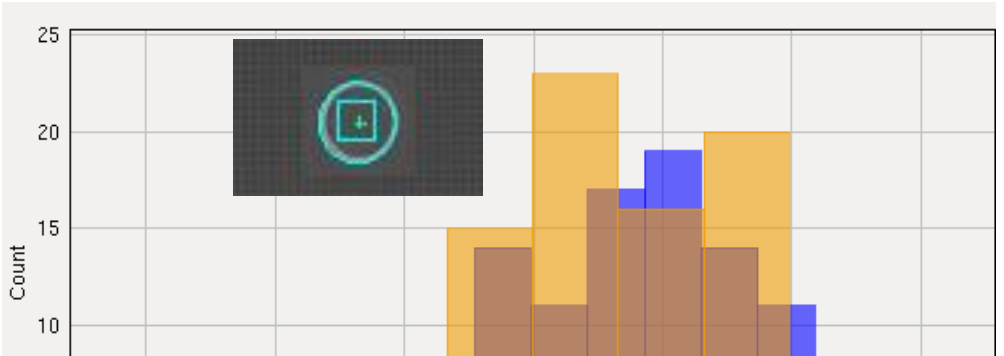
NHanced SEMICONDUCTORS

Driving Die-to-Wafer Progress

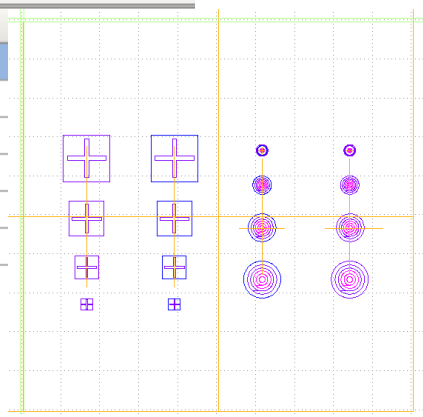
- The BESI Datacon 8800 CHAMEO ultra plus AC D2W bonding system that can reach >200nm of accuracy for each bond.
- To reach this level of accuracy the tool has demanding requirements that need to be fulfilled like:
  - Advanced tooling for the tool
    - Time and Cost
    - Plasma singulation needed
  - Specific types of key patterning and placement
    - Clear field
    - DRC waivers
  - Fiducial material design
    - Contrast
  - Film frame picking



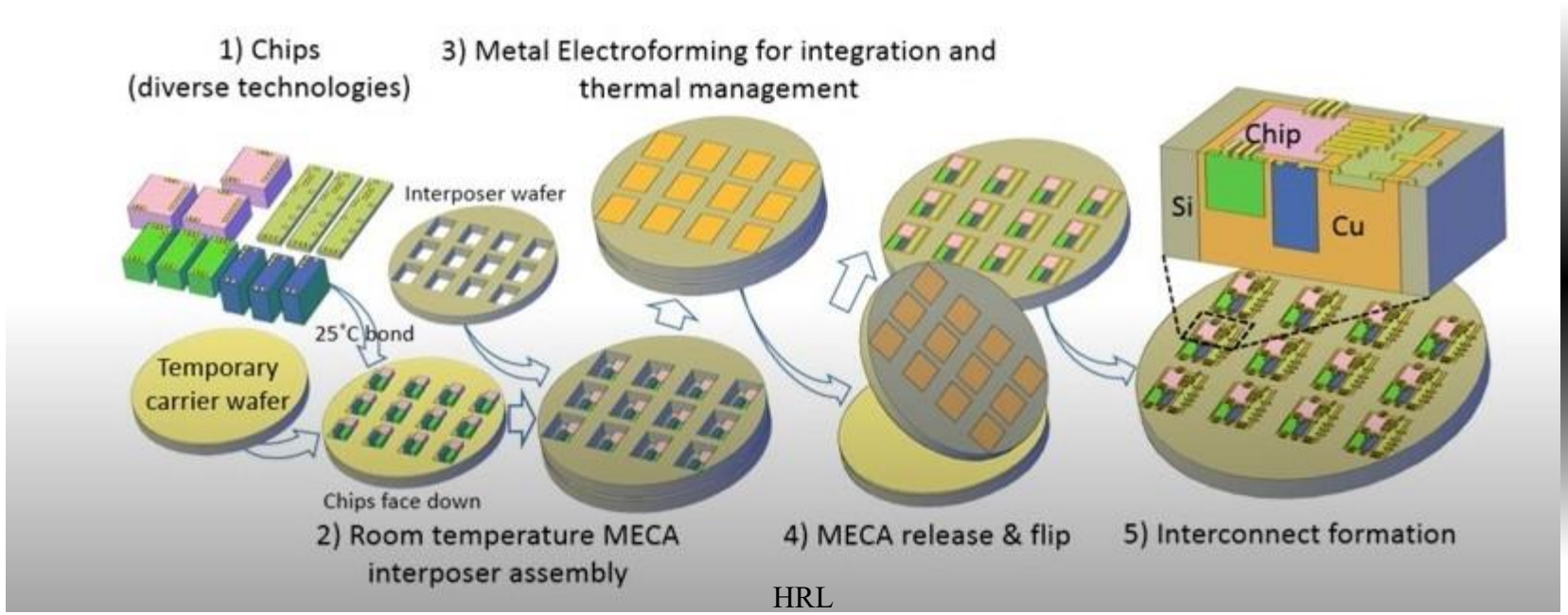
First Articles



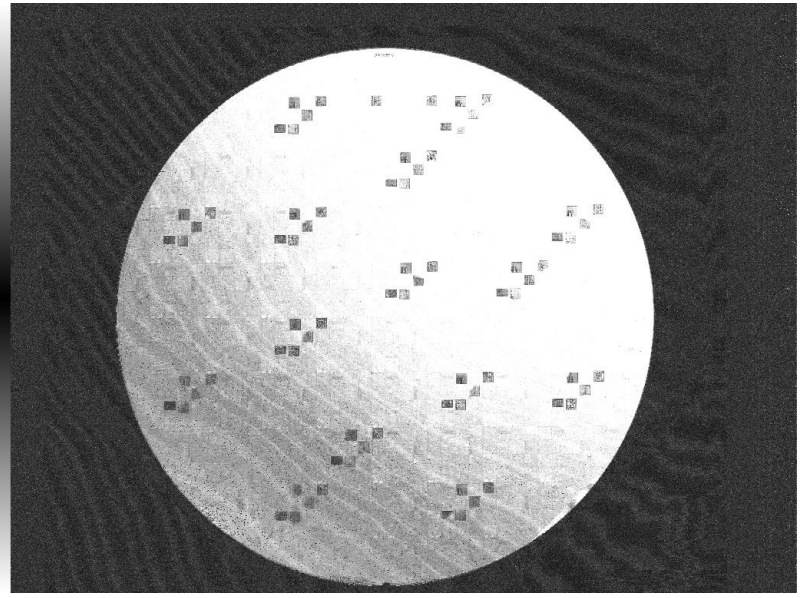
	X	Y
Mean	218.8099 [µm]	112.4263 [µm]
Minimal	218.7587 [µm]	112.3465 [µm]
Max	218.8466 [µm]	112.4791 [µm]
Range	0.0879 [µm]	0.1326 [µm]
Deviation (1 sigma)	0.0186 [µm]	0.0254 [µm]
Deviation (3 sigma)	0.0558 [µm]	0.0763 [µm]
Success rate [%]	100.0 %	



AP Cornerstones: Embedded 2.5/3D — Wafer Reconstitution

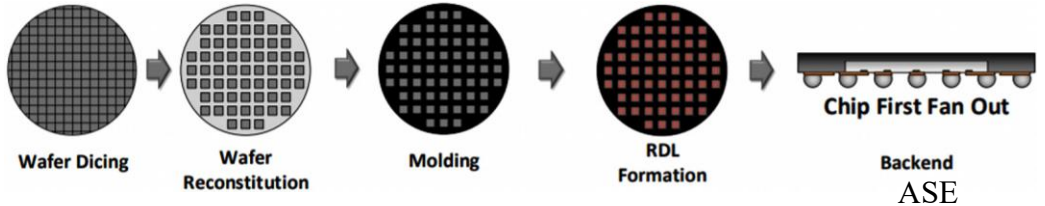


HRL



Wafer reconstruction and adaptative substrates provide additional flexibility and next level packaging alternatives.

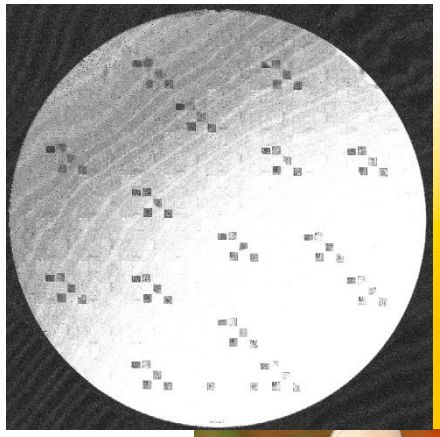
DECA Technologies

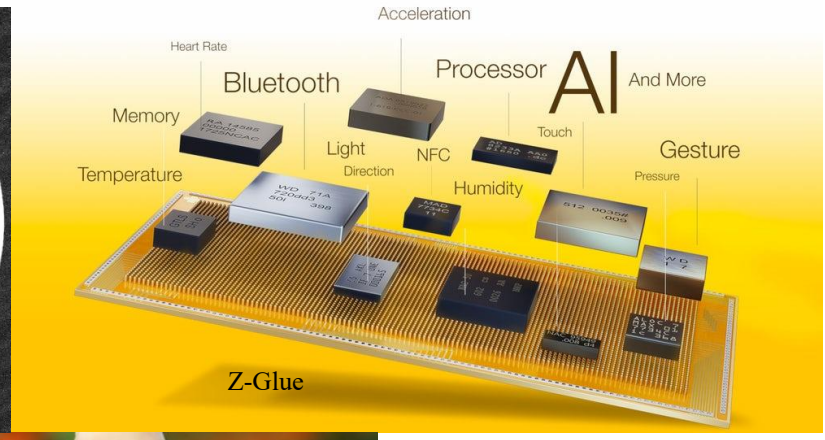


ASE

AP Cornerstones: Chiplets

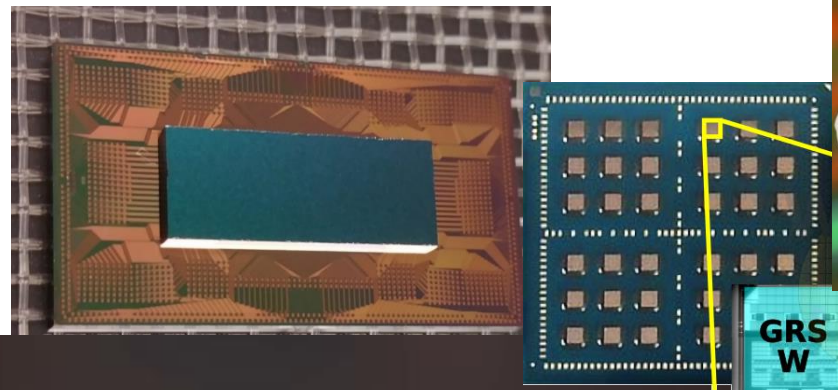
- Provides:
  - Best of Class Everything
  - Easy retargeting
  - Lower risk
  - IP reuse
  - Lower cost

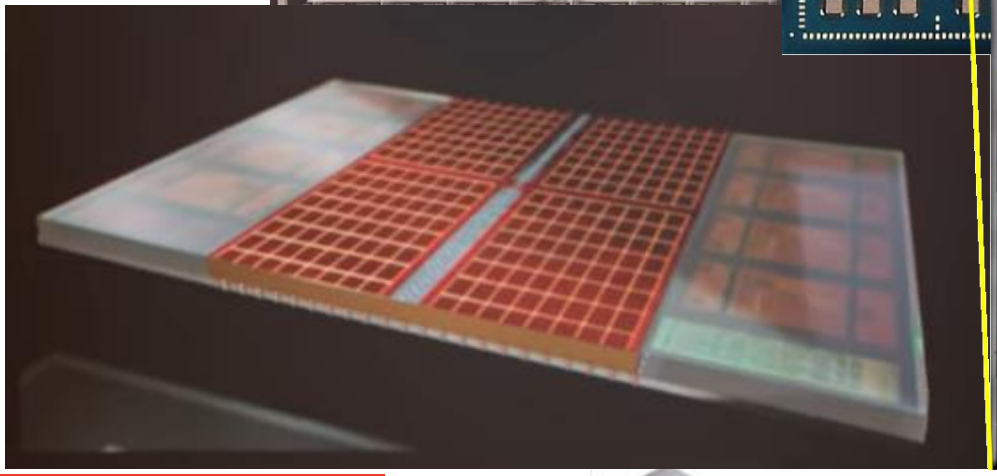




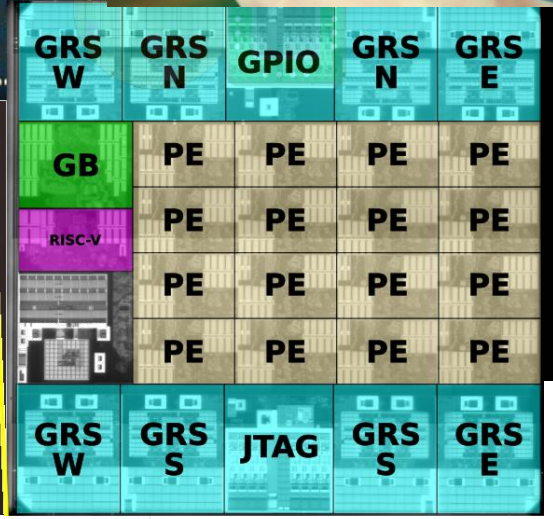
Z-Glue

Intel





AMD



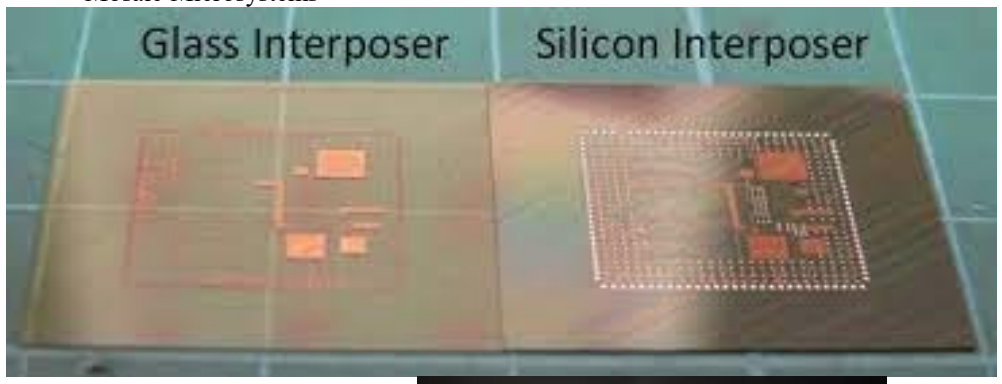
Intel

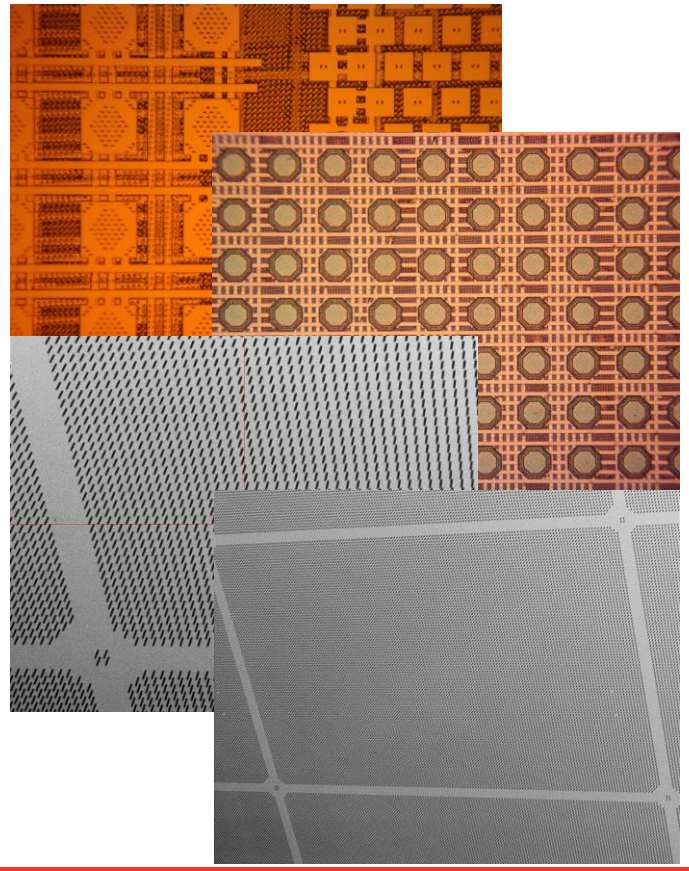
nVidia

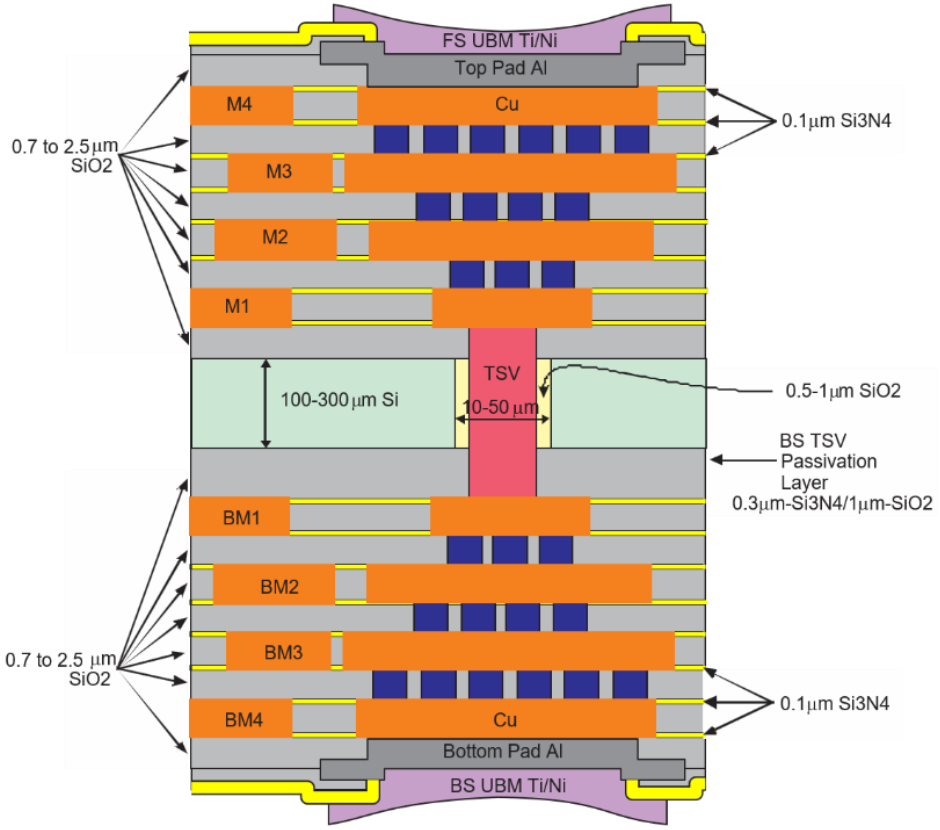
AP Cornerstones: Interposers

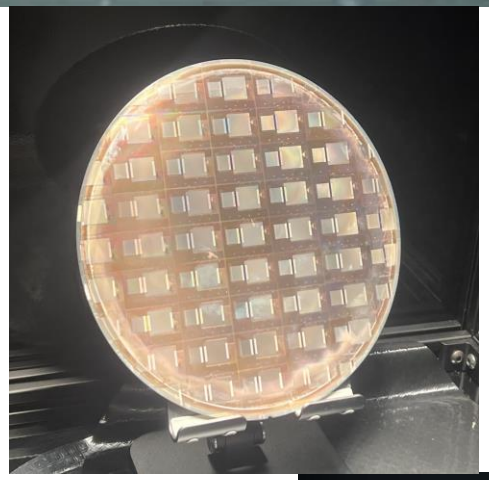
- Up to full wafer scale interposers
- HP 2um thick wiring is standard
- 4um, 6um, 10um, layer options
- Embedded decoupling caps and 12 wiring layers coming
- Optical waveguides

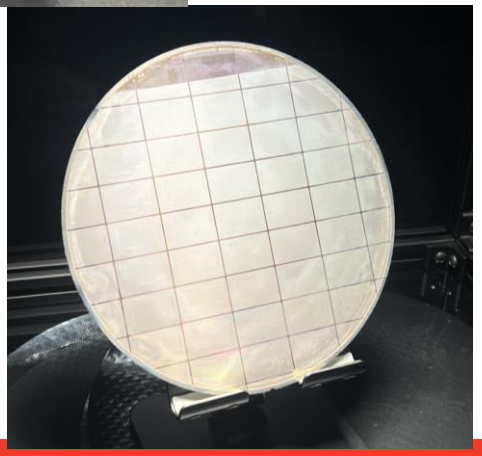
Mosaic Microsystems











NHanced SEMICONDUCTORS

Neutronix NxQ 8008, 8012, 8300

- I-Line 1X Proximity/Contact Exposure
  - Alignment Stage utilizes the latest in linear motion technology
  - Substrate Flexibility
    - Up to 3mm thick.
    - Up to 1.0 Kg substrate payload.
    - Si, Glass, Ceramic, Flexible.
    - Ø 100 mm to Ø 300 mm
    - Round, Square, Irregular.
  - Backside with IR imaging
  - Print Resolution
    Proximity 4 um at 20um gap
    Soft Contact 3 um
    Hard Contact 2 um
    Vacuum Contact 1 um
  - 0.25um 3-Sigma overlay (Hard contact)

Neutronix NxQ 8008M

Why Are We Headed To Low/Medium Volume Manufacturing?

- Transistor cost is increasing
  - To reduce cost, we need to sell the consumer fewer transistors
  - Most semiconductor devices have the kitchen sink
    - NRE is high so we can't target markets
- Chiplets offer reuse – effectively $0 NRE
- Advanced packaging NREs run ~100x less cost than lead edge node NREs
- Chiplet to chiplet power and delay is competitive with on die
- Chiplets can target markets – use only necessary transistors

→ Low NRE → Niche Market → Fewer Transistors → Lower Cost Composite Device

Moore's Law for the Next Decade

Challenges

- Litho magnification errors
  - ±10ppm fab to fab
- Litho runout
  - Layer 0 error
- Litho for 50mm, 75mm, 100mm wafers
  - Fine line
  - Edge roughness
- Stress management
  - >20um dielectric stacks
- Temp bond materials
  - TTV
  - Working temperatures
- IR losses
- High $\Delta i/\Delta t$
  - Inductance

All Jigsaw Puzzles

The Balancing Act

- Process Mix
  - Johnson's Figure of Merit
- Voltage, I/R Drop
  - Embedding decoupling
- Temperature Sensitivity
  - Photonics
- Power Dissipation
  - Cooling
    - Liquid
    - Diamond
- The more unique materials, - the greater the complexity
  - ***CTE Mismatch***
- Reproducibility at Low(er) Volumes
  - Yield

Janus Henderson

Foundry 2.0
So, Are We There Yet?

Mostly…

- ✓ EDA has made great strides
- ✓ Bonders are accurate and fast
- ✓ Standards are at least framed
- ✓ Chiplets exist in silos
- ✓ True heterogenous integration is field proven
- ✓ We have a “Tool Box”
- ✓ Product is shipping

AI, Hyperscaling, Photonics now fully embrace AP

It is all about a new System Level Moore’s Law

Valley of Fire Road — Valley of Fire State Park