The Evolution of Electronics Packaging to Chiplet Architecture

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Acknowledgements

The Future of Electronics Packaging Is Chiplet Architecture

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Introduction

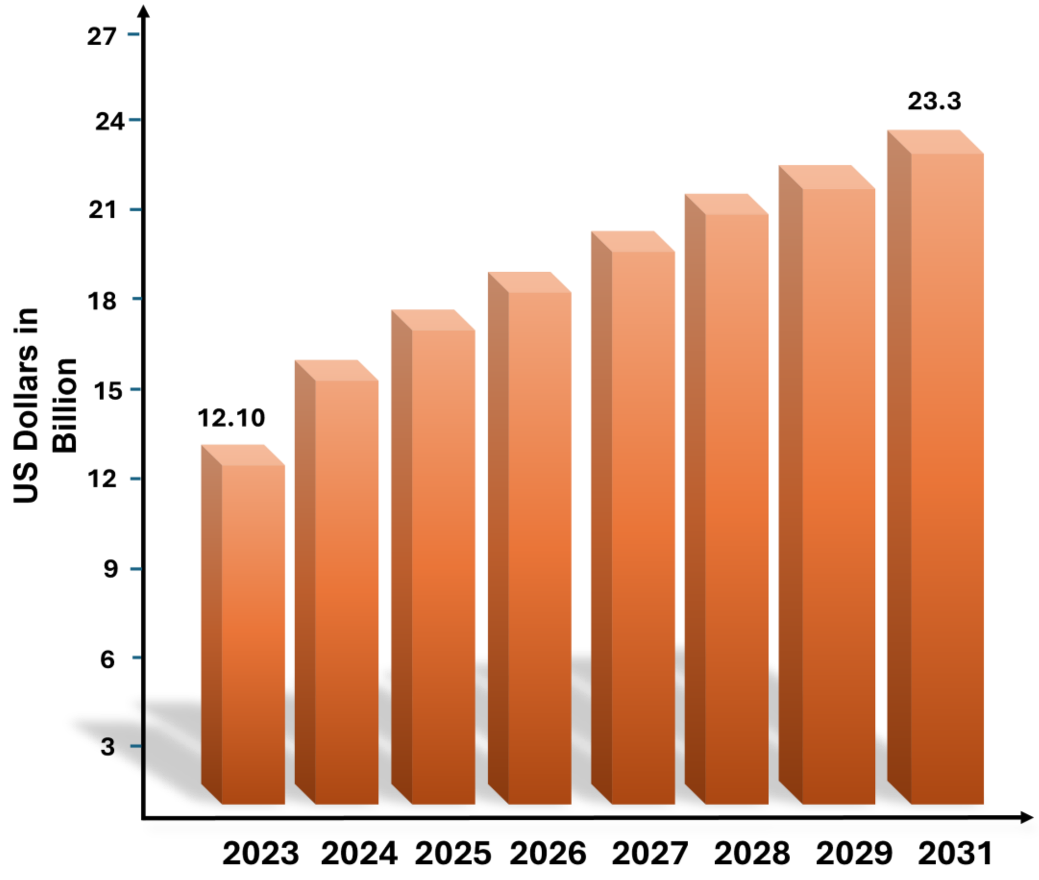
- Evolution of semiconductor technology has exposed the limitations of traditional monolithic SoC designs.
- Transistor scaling yields diminishing returns.
- Industry is transitioning toward a chiplet-based architectures.
- Disaggregation improves design flexibility, supports heterogeneous integration and enhances scalability.
- This approach enables optimization of power, performance and area across functional domains.

Introduction

- Chiplet integration requires interconnect technologies that support high density, low resistance and capacitance, as well as minimal thermal and mechanical tress.
- Conventional methods, such as, micro bumping and thermal compression bonding face significant limitations at sub-10um pitches.
- These constraints have driven the emergence of hybrid bonding as the next generation of interconnect solution.
- Hybrid bonding eliminates intermediary layers, reduces interconnect height, minimizes parasitic effects and improves thermal and mechanical integrity.

Current State of Global Hybrid Boding Technology

Hybrid bonding has emerged as a leading solution to scales to finer pitches below 10um, enabling integration with strong electrical, mechanical, and thermal continuity through a co-optimized process flow.



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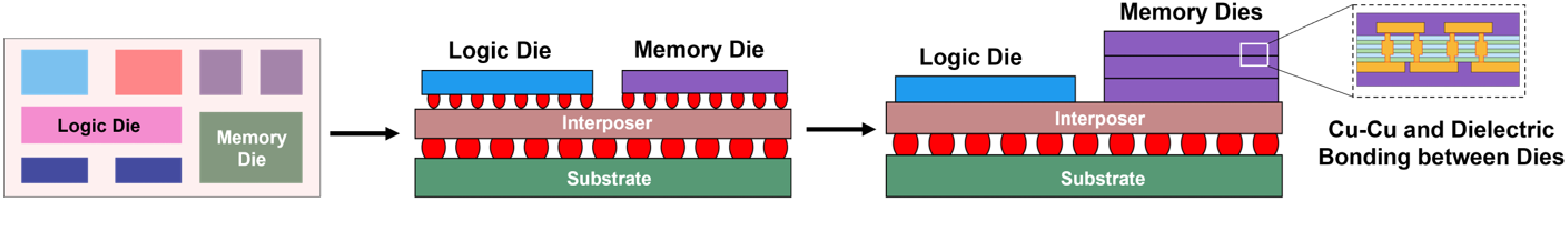
Transition of Chiplet Architecture from SoC to 2.5D and 3D Advanced Packaging



Chiplets Embedded in SoC

Chiplet connected via Microbumps

Chiplet connected via Hybrid Bonding

Comparison of Hybrid and Micro-Bump Bonding

Property	Hybrid Bonding	Micro-Bump Bonding
Minimum Pitch	<10 µm [14]	≥30 µm [15]
Interconnect Stack Height (Z-height)	≤5 µm [10]	20–30 µm [16]
Contact Interface	Cu–Cu and oxide–oxide	Solder-based
Thermal Interface Resistance	~1.2 mm^2·K/W [17]	~8–15mm^2·K/W [18]
Current Density Handling	>8.9 MA/cm^2 [19]	~1.5–5 MA/cm^2 [20]

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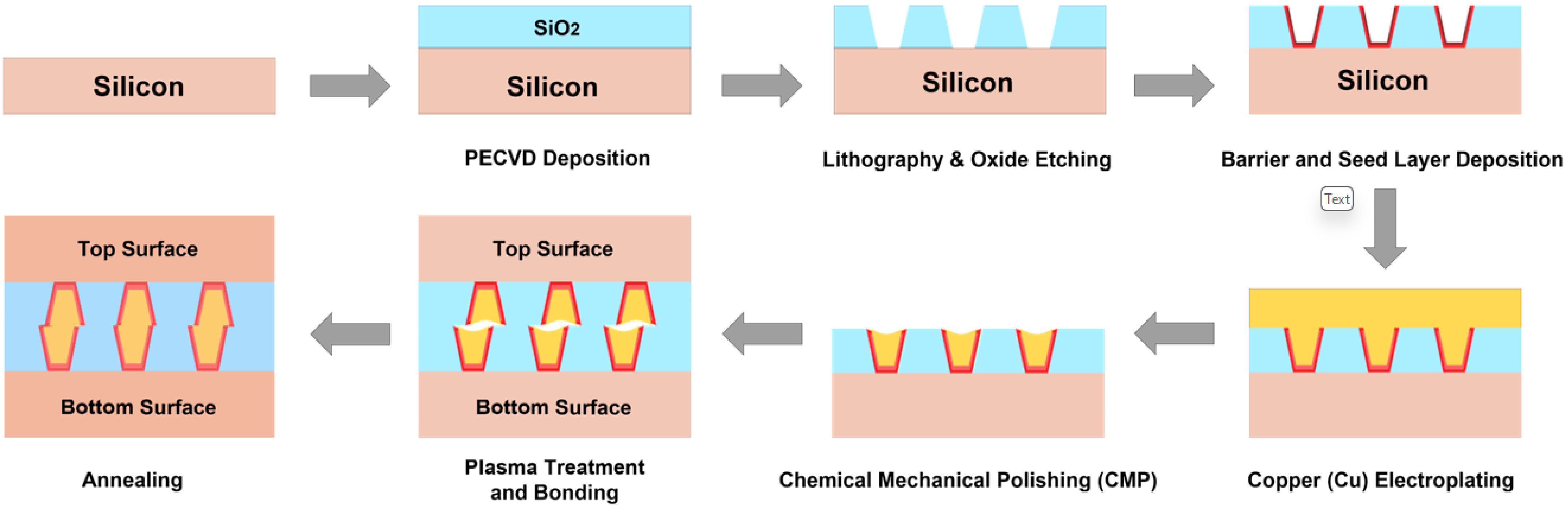
Hybrid Bonding Process Flow



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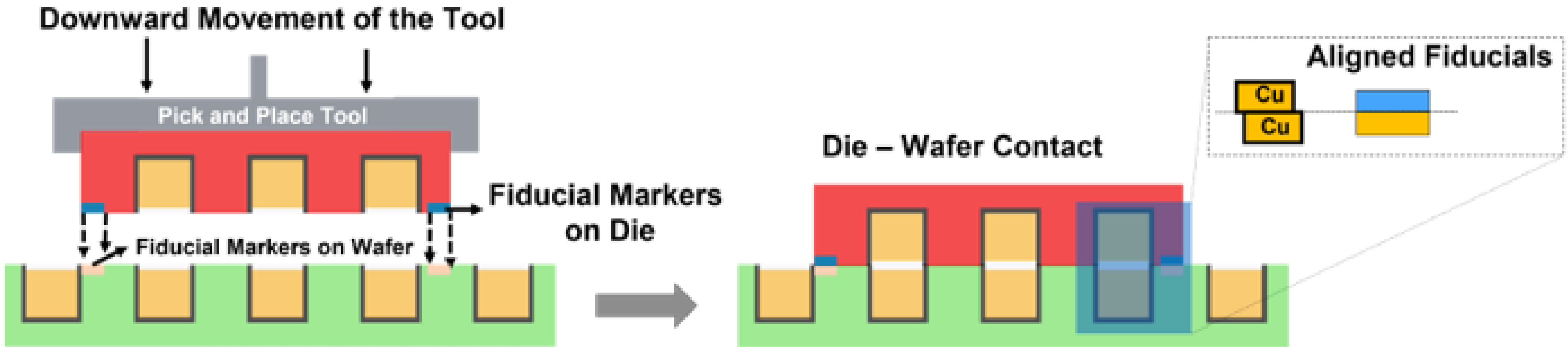
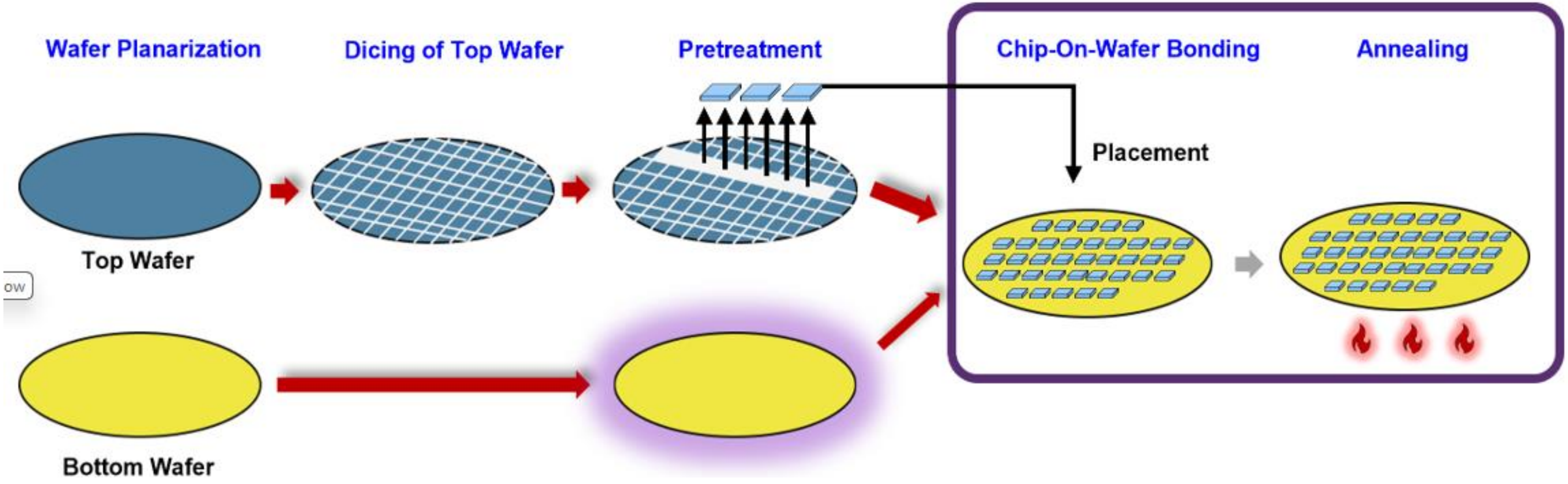
C2W Assembly



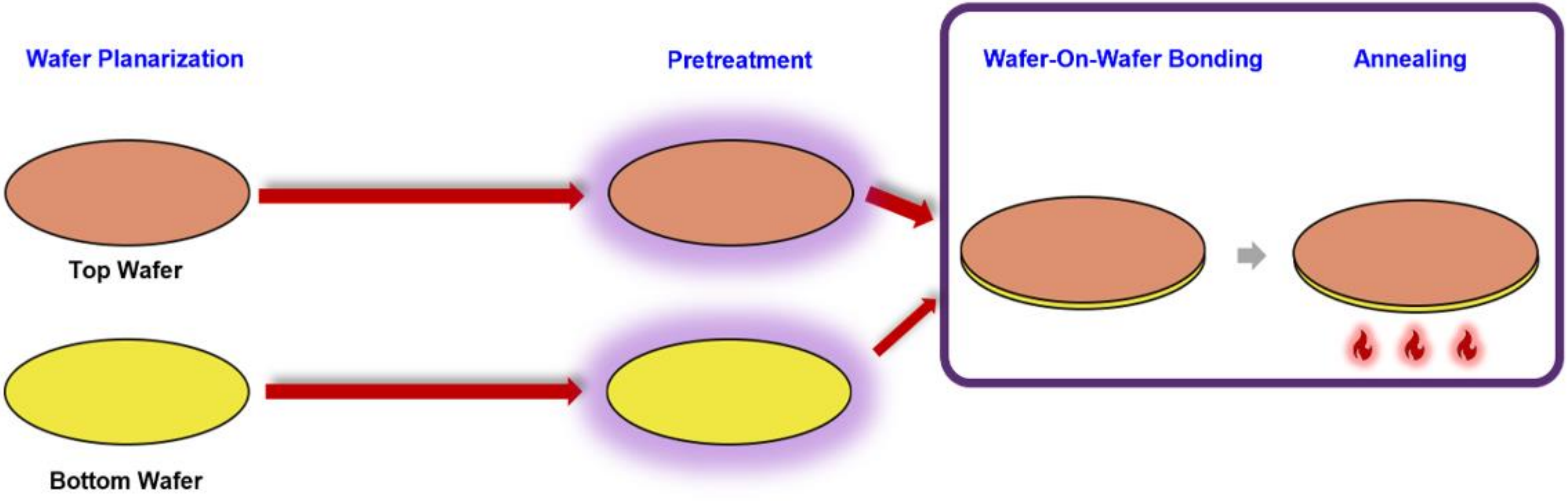
Comparison of C2W and W2W Bonding

Metric	C2W Bonding	W2W Bonding
Alignment Method	Sub-micron alignment via vision systems; adaptive placement of KGDs	Global wafer-level alignment using stepper systems or optical marks
Throughput	Moderate; limited by serial die placement and alignment overhead	High; entire wafer bonded in batch, suited for volume manufacturing
Yield Dependency	Favorable for heterogeneous integration; yield preserved by using only KGDs	Yield is sensitive to wafer-level uniformity; defects or non-uniformity
Die Uniformity Requirements	Critical: each die must meet planarity and thickness targets to ensure reliable interconnect formation	Important; global Wafer planarity managed via pre-bond CMP and thinning uniformity
Equipment Complexity	High; advanced pick-and-place tools with real-time metrology and surface correction	Moderate; streamlined equipment flow with fewer moving components
Application Examples	High-performance compute tiles, custom logic integration, AI/ML chiplet modules	HBM stacks, image sensor arrays, logic-memory vertical integration with high Wafer yield

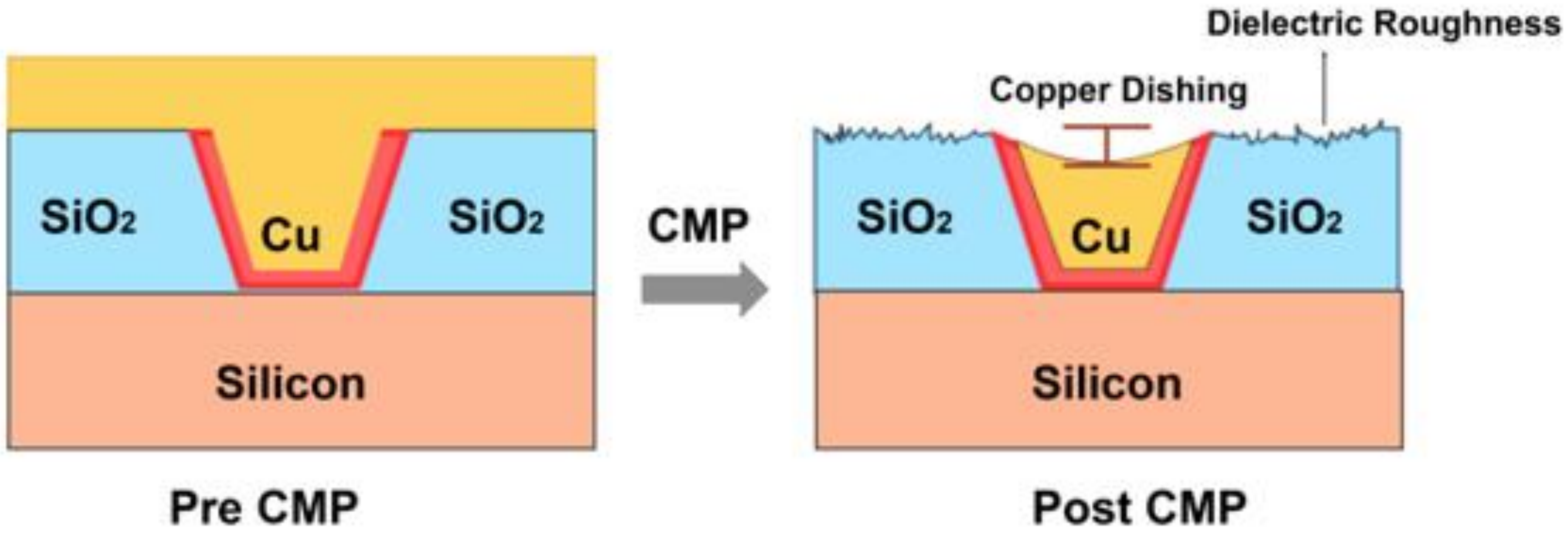
C2W Process Flow



W2W Process Flow



Individual Cu Pad level observation of Dishing and Dielectric roughness induced by Improper CMP Process



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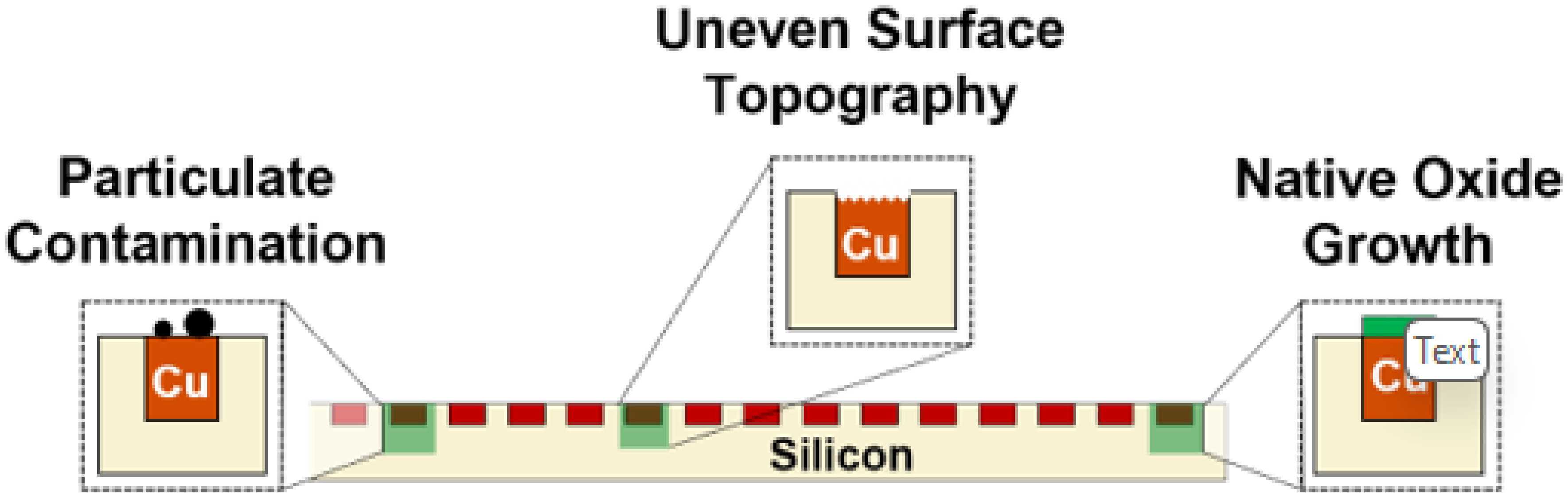
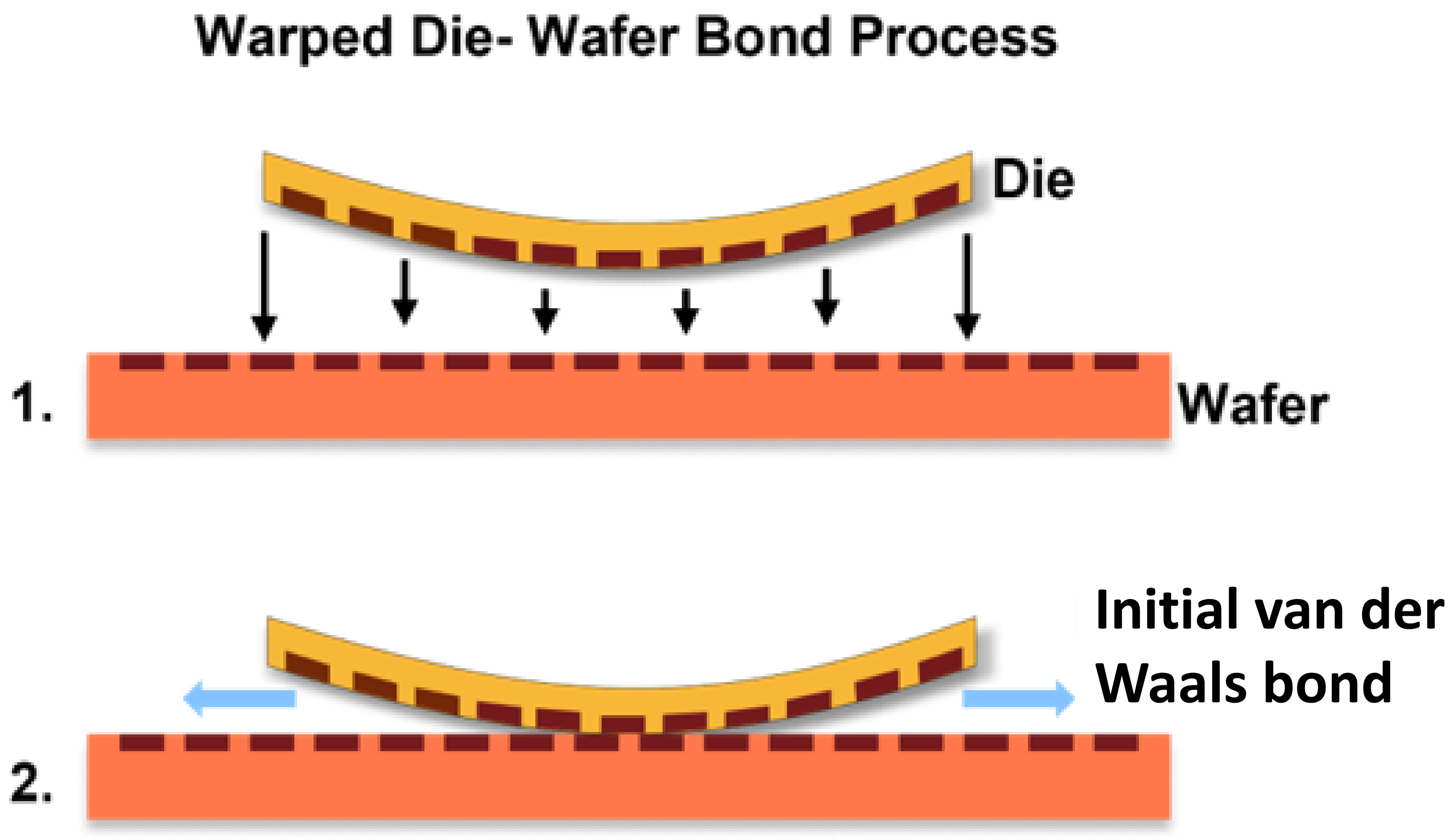
Defects Observed at Sub-Micron Pitches

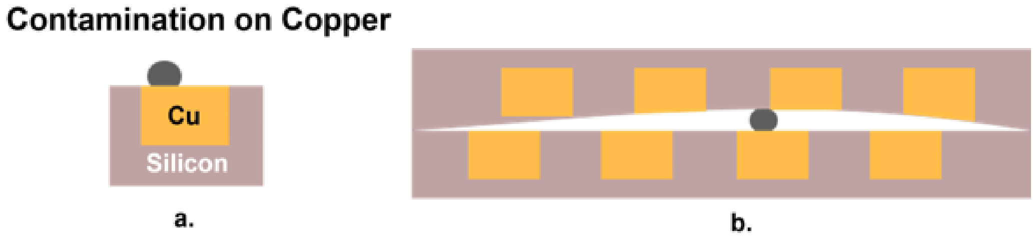


Warped Die-Wafer Bonding Process showing a smiley thin die wafer bonding with a flat wafer by the initial van der Waals bonding forces



C2W Challenges

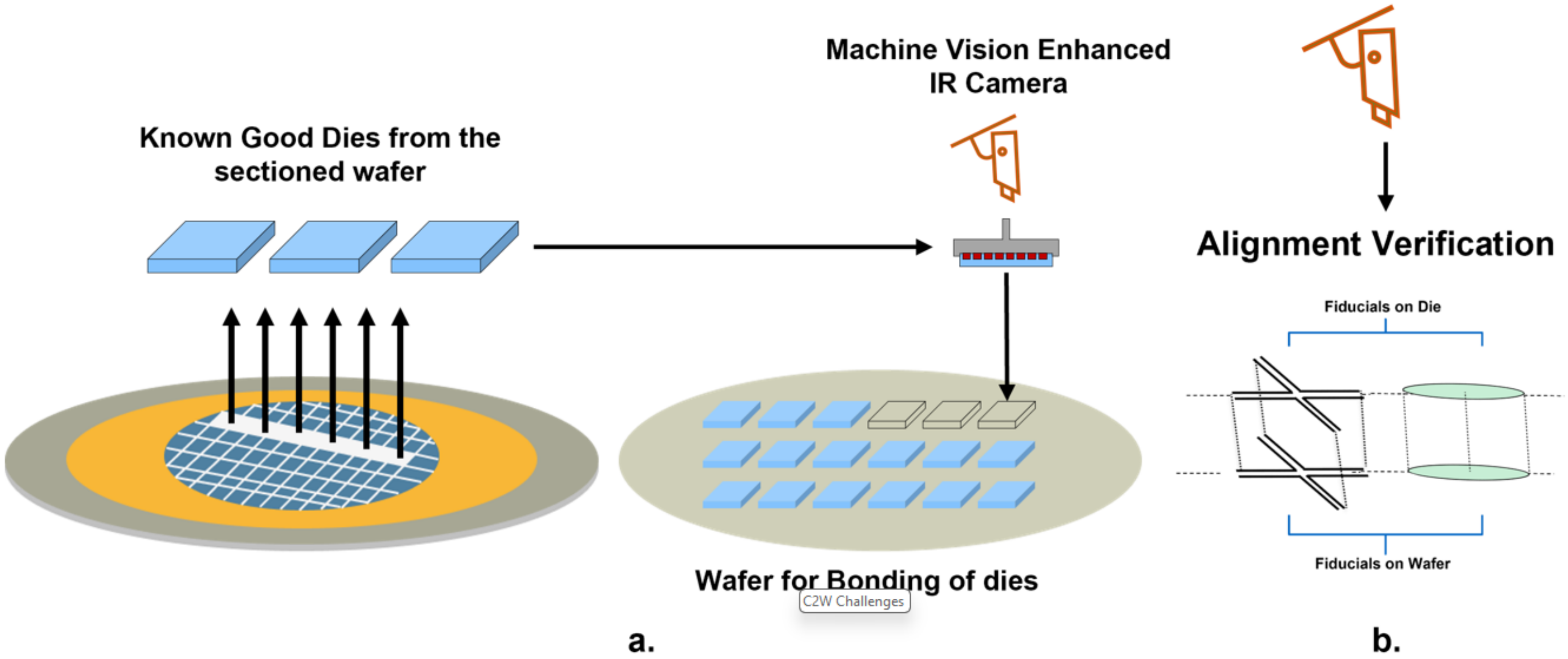
- Edge effects in die placement
- Precision in die placement
- Recess control and pad height variatic
- Surface cleanliness and particle control
- Post-bond alignment drift
- Chiplet-level distortion through the die



a. Close View of contamination on top of Cu Pad post CMP and Plasma Cleaning. b. Microscopic View of Air gaps created by the contaminated particle on the post-bonding interface

C2W Challenges

Removal of Dies from the sectioned Wafer and placement on the new Wafer for C2W Integration. b. Machine vision enhanced IR Camera for Ensuring and Verifying a Precise Fiducial alignment



Recent Developments Towards Solving the Challenges

- Surface planarization and bond interface preparation
- Adhesive layer integration for void mitigation
- Misalignment detection and correction techniques
- Control of chiplet bonding during attachment
- Carrier-based and organic layer management
- CMP uniformity control
- Vacuum-controlled bonding environments
- AI/ML for defect prediction and process optimization

Foundry 1.0

- Current semiconductor business has been focused on driving smaller transistors.
  - High development cost
  - High capital cost
  - Long development times
  - Expensive design tools
  - High risk

- Twilight of Moore's Law

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A New Semiconductor Industry Paradigm

Foundry 2.0 –

A Finishing Foundry that takes the standardized building blocks from traditional semiconductor manufacturers and uses advanced packaging and additive manufacturing to create highly customized components with superior performance targeting small and medium sized markets.

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Foundry 2.0 Opportunity

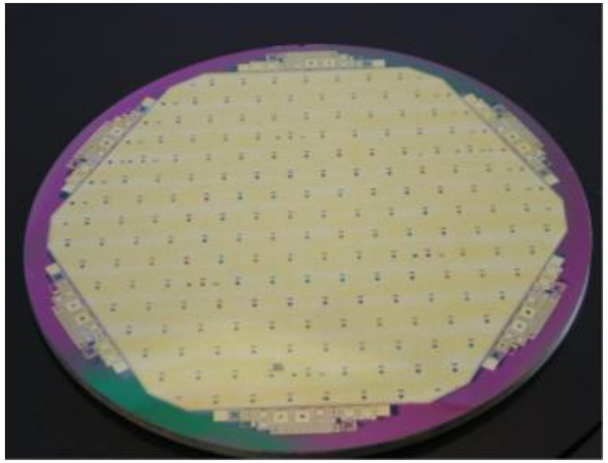
- There are no de facto winners
  - Intel, AMD, Xilinx, Marvell, -- Currently IDM driven but nascent
- Low capital costs
  - More than an order of magnitude lower capital costs
- Supports low and medium volume flows – High mi
  - USG, startups, large swath of industry
    - More cost effective
  - Competition is FPGAs 10x to 50x lower component cost
- IP centric Knowledge based value
- Phased approach works well
- Complementary to Foundry 1.0
  - Partnering Customers, Capital, Pile-on

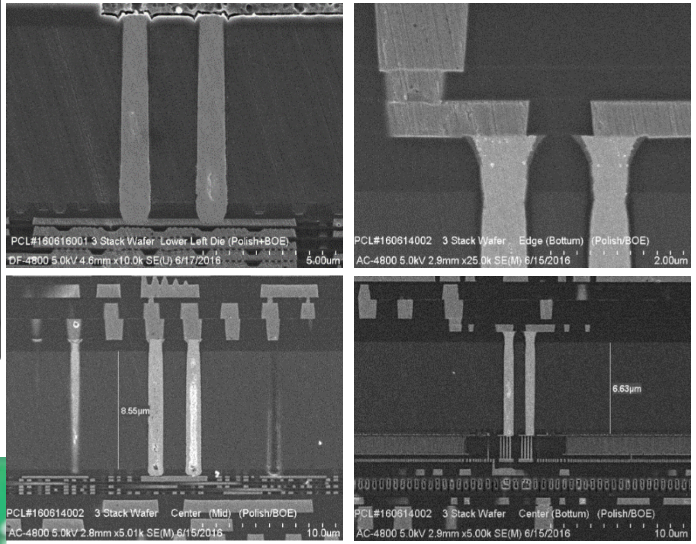
Changing to a High-Mix, Lower Volume Manufacturing Model

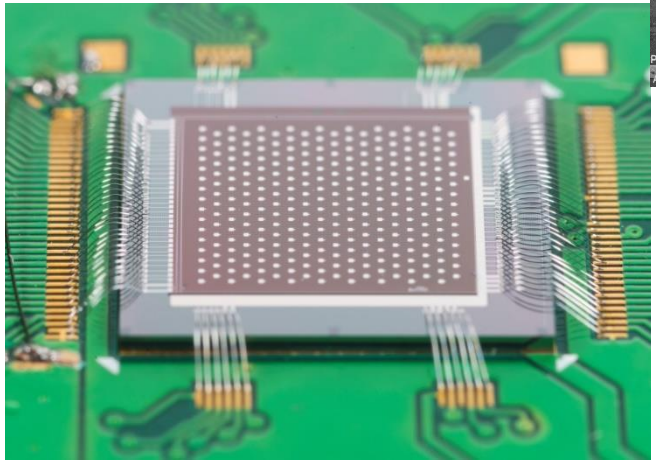
Small/Medium Scale – High Touch Manufacturing

- 2.5/3D Advanced Packaging
- Si Sensors
- Commercial Development
- Mil-Aero Development and Manufacturing
  - Full BEoL
    - Niche BEoL Processes
    - Cu, Ni, Al, +
  - Split-Fab
  - High k-caps
  - ReRAM
  - 3/5 and LiNbO3 integration
  - Thick Wafer & Thin Wafer Processing
- ISO9001

- Target market is customers needing
  1 to 5000 wafers per year







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High Volume Manufacturing – Customized At-Scale Manufacturing

- 2.5/3D Advanced Packaging
  - Hybrid Bonding
  - Customize Metal Stack
- Interposers
  - Silicon
  - Glass
- Target market is customers needing 500 to 50,000 wafers per year

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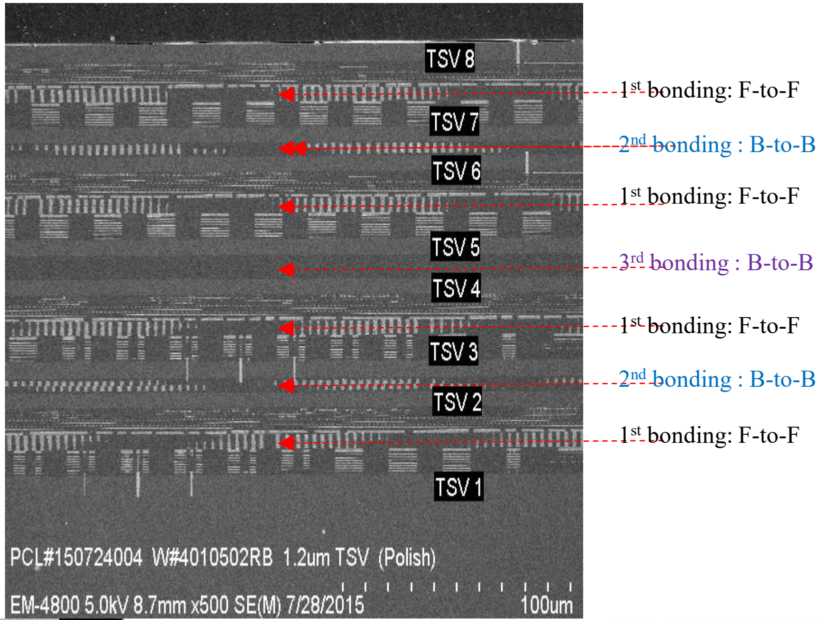
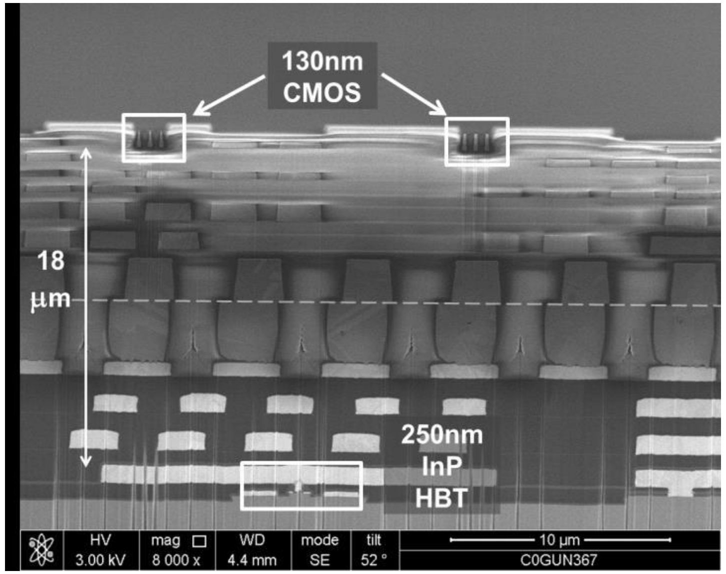
AP Services: Bonding

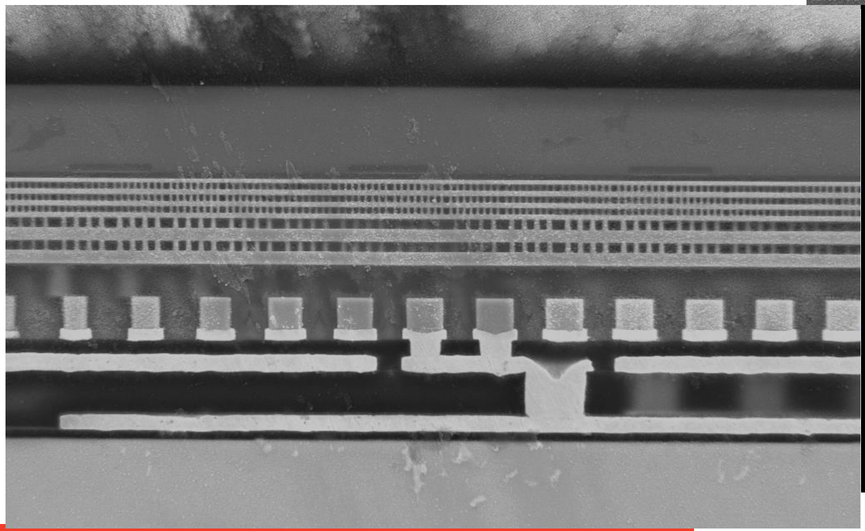
- High maturity
- Up to 20 tiers
- True heterogenous with micron scale interconnects
- Die-to-wafer, wafer-to-wafer

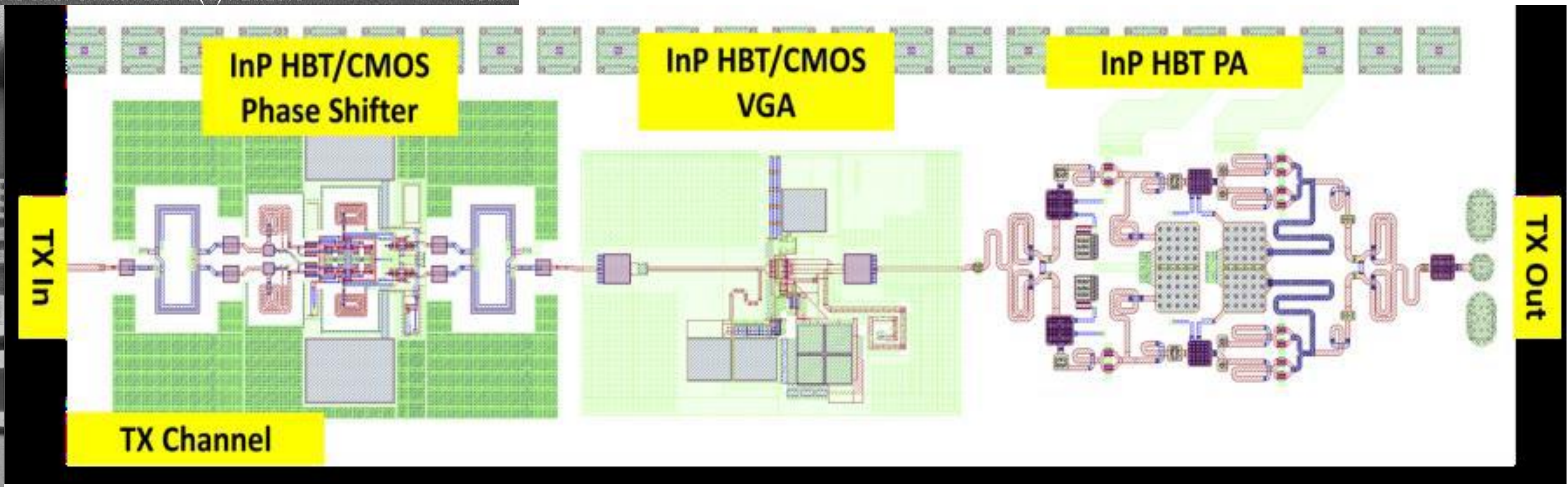




Mixed Materials

Best of Class





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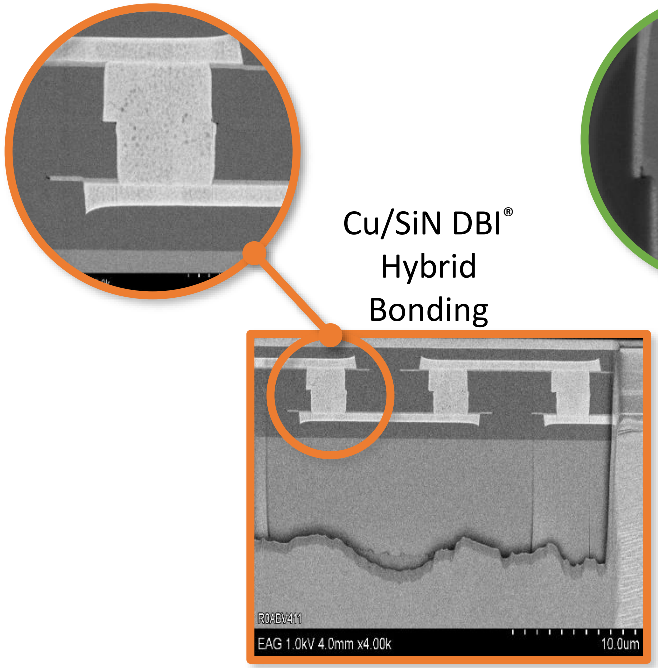
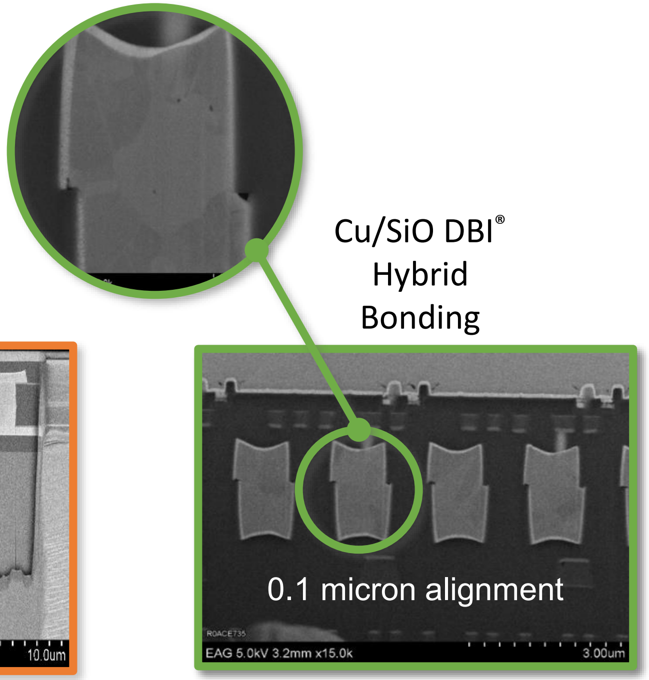
Hybrid Bonding Interconnect Pitch Scaling

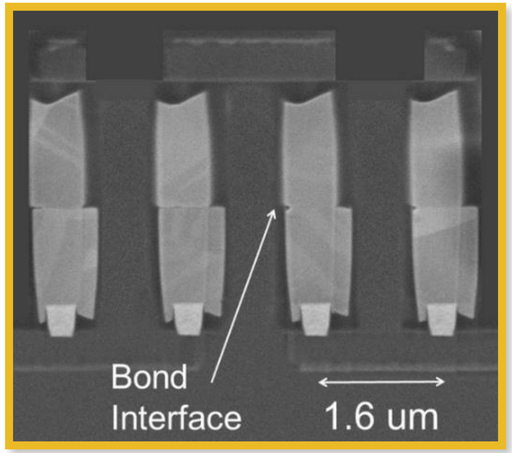


10 μm DBI® pitch, 300℃



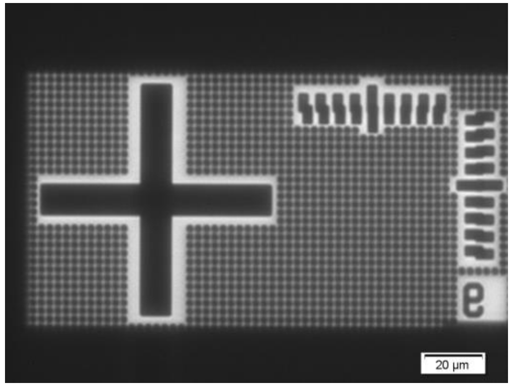
1.9 μm DBI® pitch, 300℃

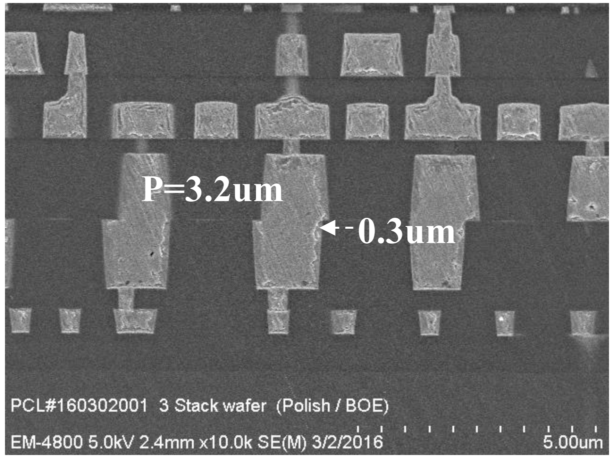
Scalable To < 1um Pitch
0.8um Pitch Demonstrated



1.6 μm DBI® pitch, 300℃

- WtoW 3sigma < ±1um misalign performance
- DtoW 3sigma < ±200nm misalign performance
- Production Minimum pitch = 2um





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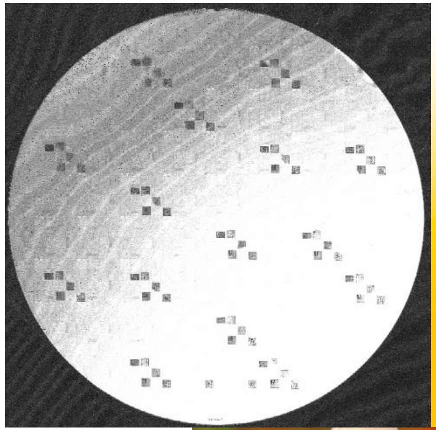
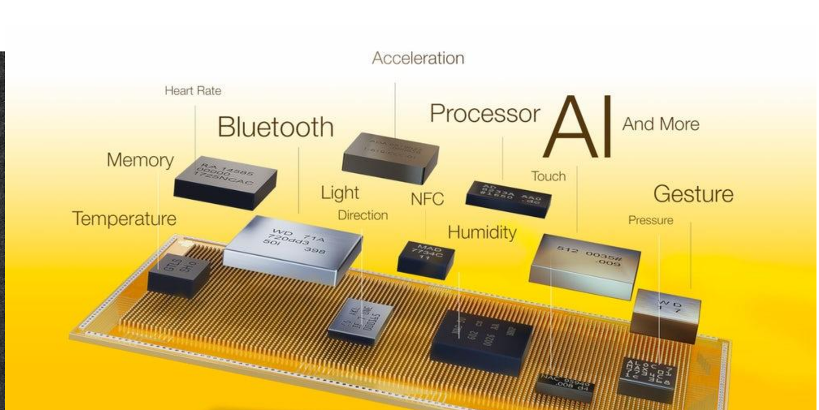
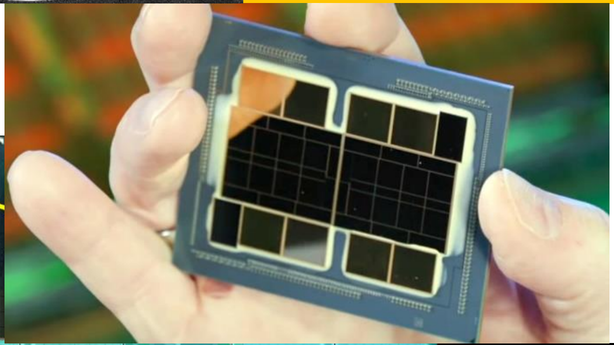
Examples of Chiplets Integration

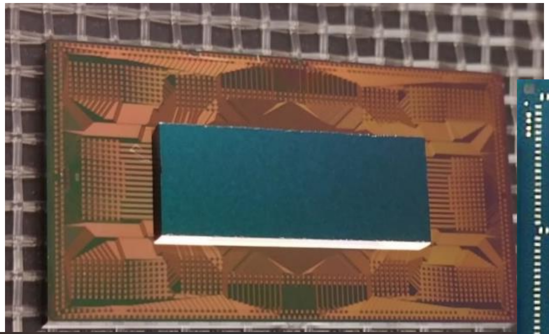
- Provides:
  - Best of Class Everything
  - Easy retargeting
  - Lower risk
  - IP reuse
  - Lower cost

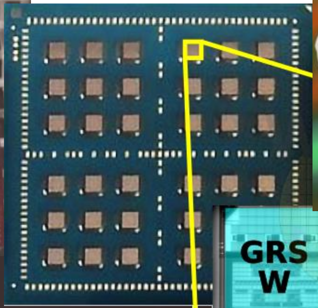


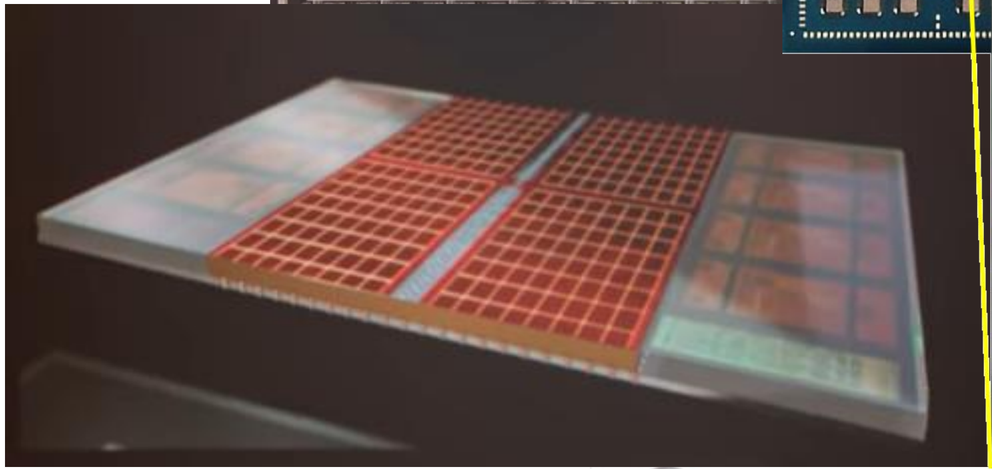


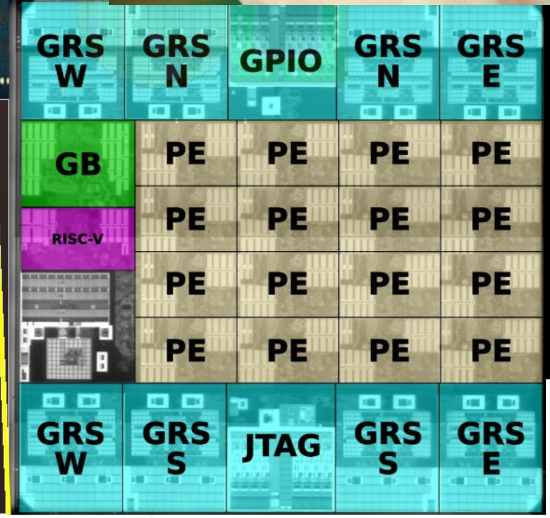
Z-Glue


Intel






AMD



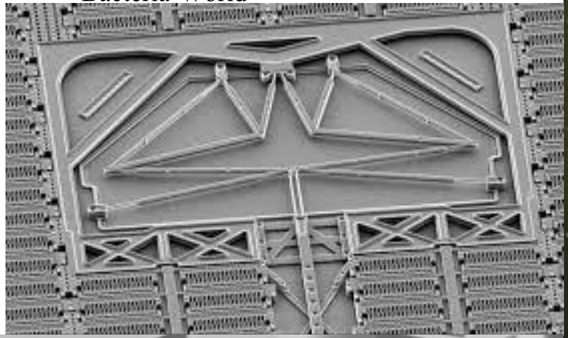
nVidia

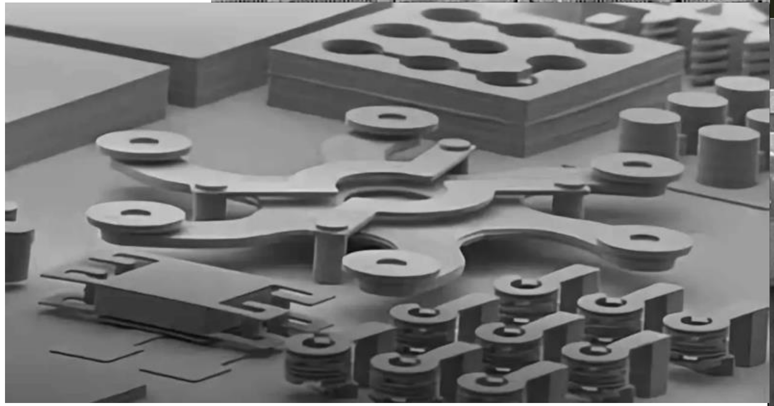
Intel

Micro-Connections and 3D Structures

MEMS + Precision Electronics

Bacteria-World





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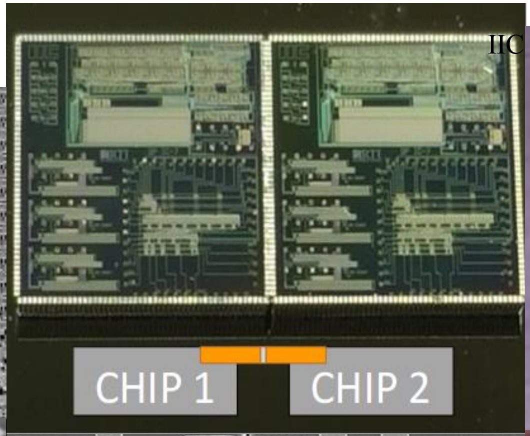

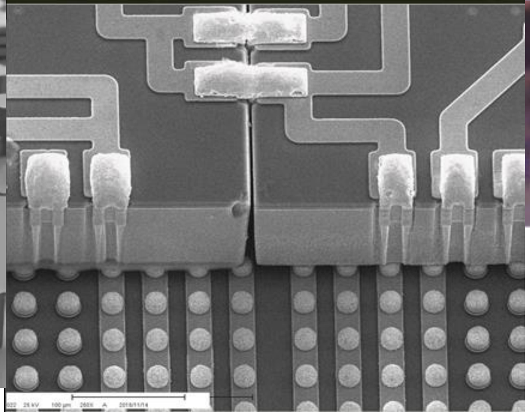

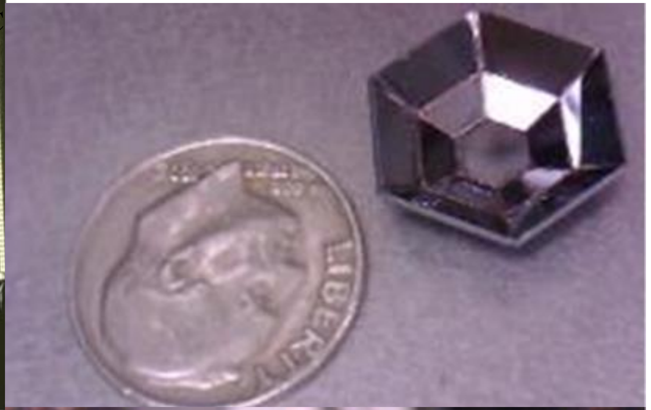

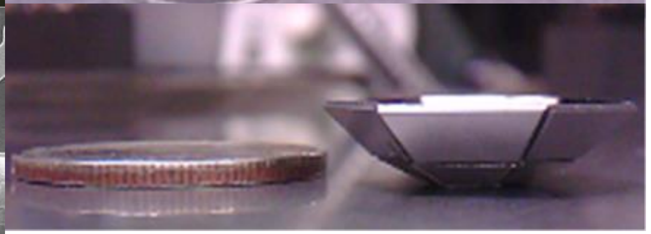

(top left) Quilt Packaging concept cross-section illustration & image of a post-reflowed QP CMOS quilt; (bottom left) SEM image of quilted chip-to-chip seam of >10 micron width; (top right) QP-enabled miniature curved array demonstration article; (bottom right) profile view of QP-enabled miniature curved array.

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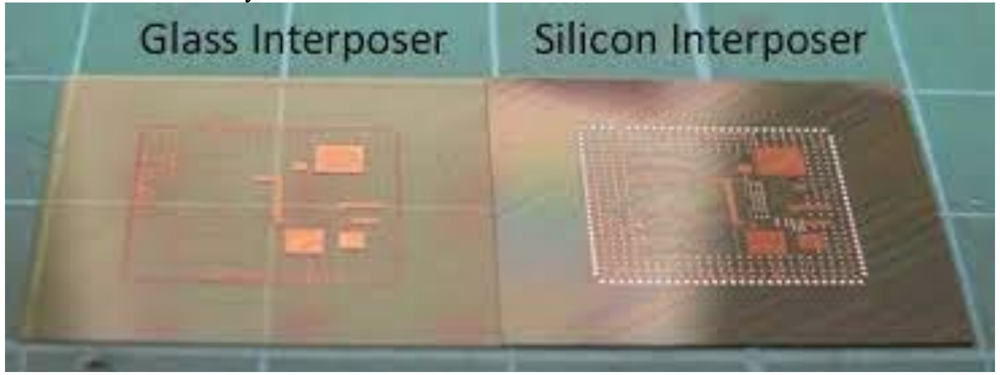
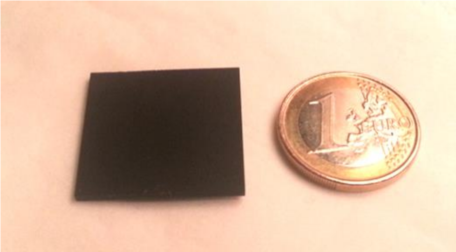
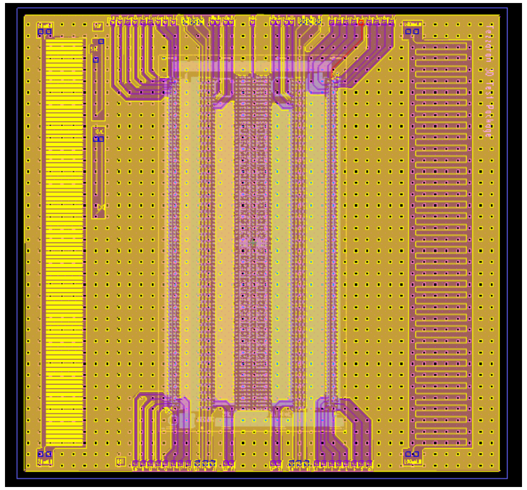
Interposers

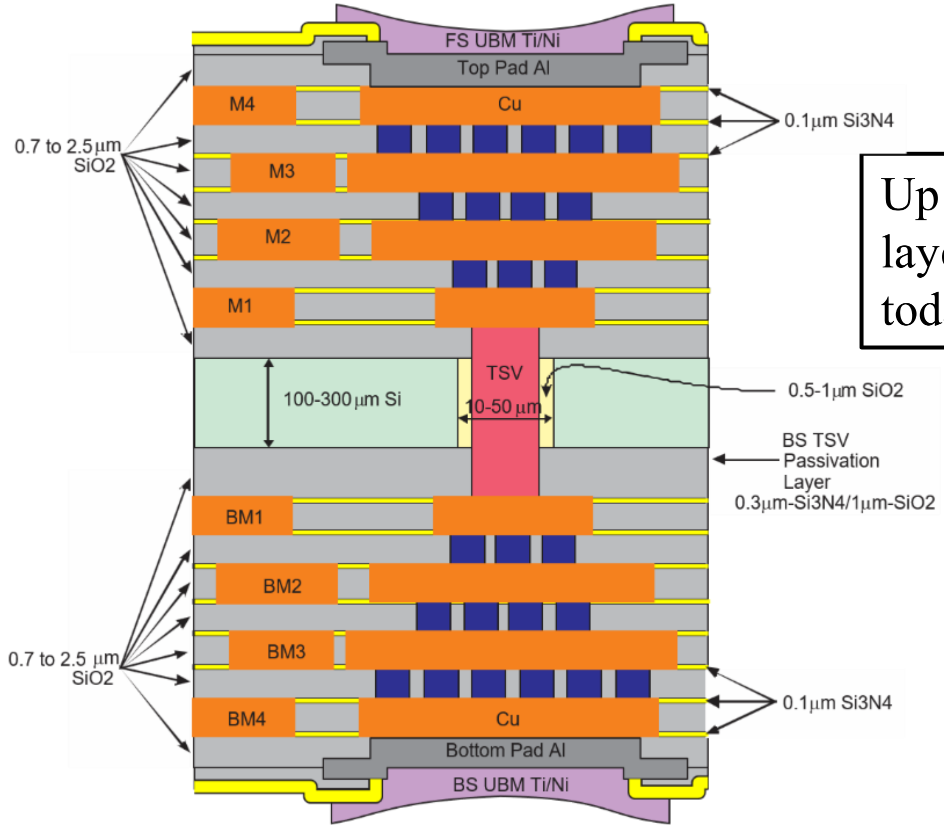
- Up to full wafer scale interposers
- HP 2um thick wiring is standard
- 4um, 6um, 10um, layer options
- Embedded decoupling caps and 12 wiring layers coming

Mosaic Microsystems

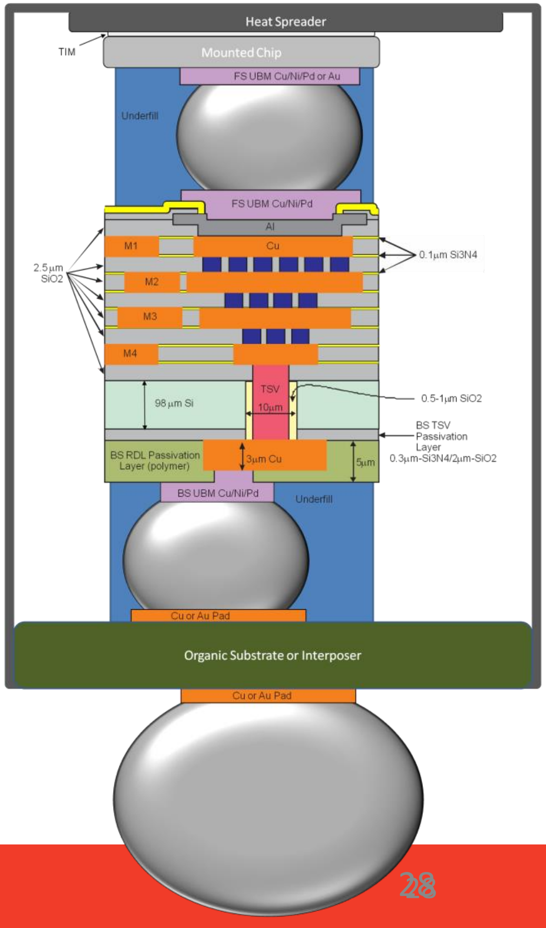








Up to 8 wiring layers available today



Future Outlook

- The transition to hybrid bonding represents not just an evolutionary step in advanced packaging, but a foundational shift in how semiconductor integration will be structured in the coming decades.
- The modularity provided by chiplets, combined with the fine-pitch capabilities of hybrid bonding, is setting a new standard for heterogeneous integration.
- One of the most impactful developments driving this shift is the growing adoption of the Unified Chiplet Interconnect Express (UCIe) standard.
- To enable this integration path, foundries are developing UCIe-compliant process design kits (PDKs) that include hybrid bonding modules optimized for thermal, power, and yield-aware floor planning.

Conclusions

- The transition from monolithic SoC integration to modular chiplet-based architecture has fundamentally reshaped the landscape of advanced electronics packaging.
- The future of hybrid bonding lies in its evolution toward bumpless, pitch-agnostic interconnects and native compatibility with open standards, such as UCIe.
- Foundry 2.0 is the future of semiconductor manufacturing for chiplet integration.
- As industry converges on modular, heterogeneous platforms, hybrid bonding will continue to be a foundational enabler.

Thank You!

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VP Business Development

NHanced Semiconductors, Inc.