Hybrid Bonding a Key Enabling Technology for Chiplet Integration

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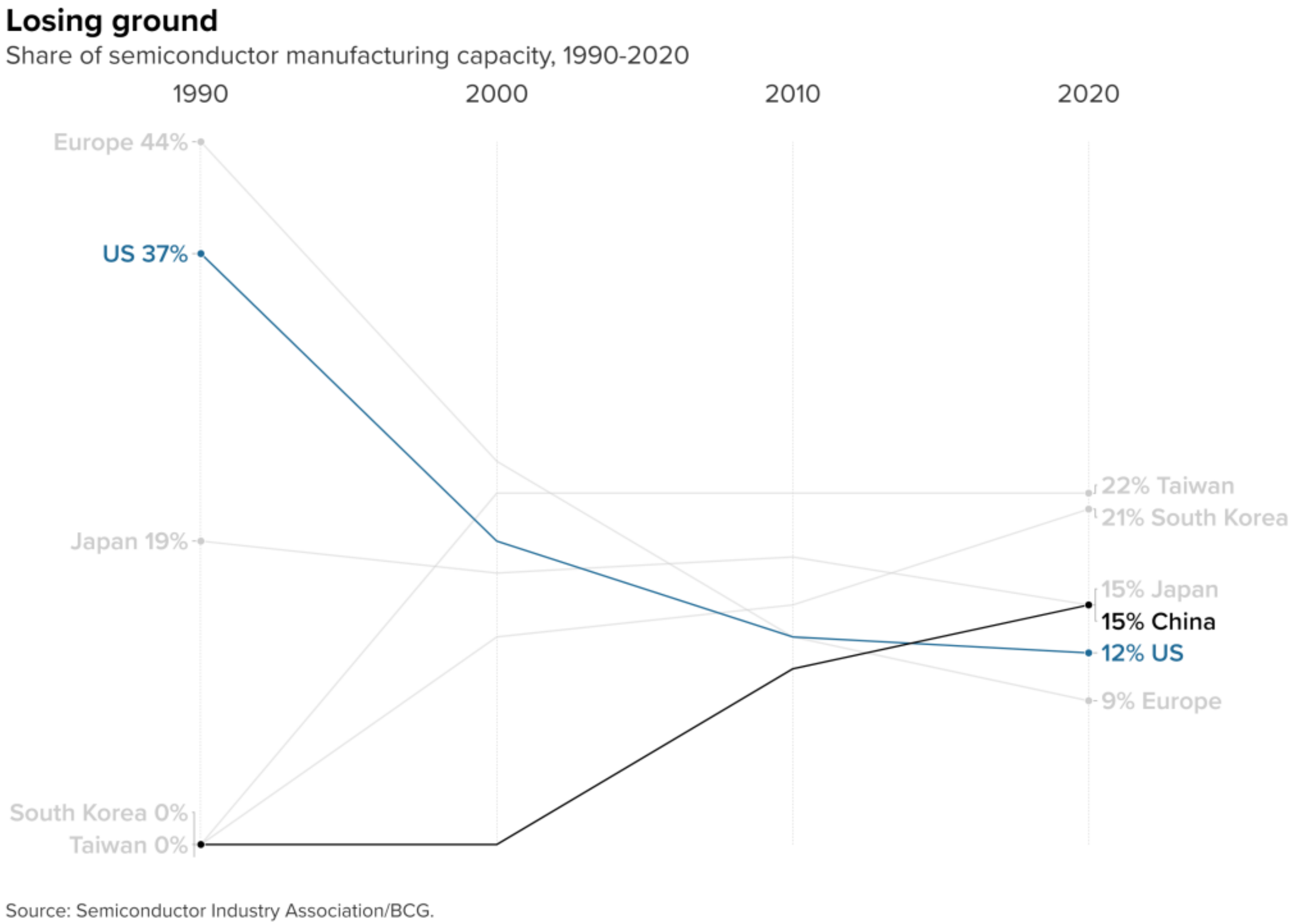
Semiconductor Mfg. Capacity



Global Landscape

North America is in a Weak Position for AP/HI

Reference: Yole 2023

Effective End of Moore's Law

Moore's Law was first and foremost a statement about economics. We could shrink transistors and build more of them for about the same cost.

- This has been the basic premise of the semiconductor industry for 50 years and was true up until the last few years.
- Today we can indeed shrink transistors further, but the cost per transistor no longer declines.

  We can get something a little more compact

  - Perhaps a little less power
  - But we pay more for these features now.

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Breakdown of Dennard Scaling

Dennard scaling, the principle that transistor power density remains constant as transistors get smaller, has been a fundamental driver of improvements in computing performance for decades. However, this scaling has slowed down significantly in recent years due to several technical and physical challenges:

1. **Leakage Current**: As transistors shrink, the thickness of the gate oxide layer decreases, leading to increased leakage currents. This leakage contributes to higher power consumption and heat generation, negating the benefits of smaller transistor sizes.
2. **Short Channel Effects**: When transistors become extremely small, short channel effects such as drain-induced barrier lowering (DIBL) and threshold voltage roll-off become more pronounced. These effects degrade the performance and reliability of the transistors.
3. **Heat Dissipation**: As transistors shrink and their density increases, the ability to effectively dissipate heat becomes a critical issue. The heat generated by densely packed transistors can lead to thermal management challenges, impacting performance and longevity.
4. **Quantum Effects**: At very small scales, quantum mechanical effects become significant. Quantum tunneling, for instance, can cause electrons to pass through insulating barriers, leading to increased power consumption and unpredictable behavior.
5. **Material Limitations**: The traditional materials used in semiconductor manufacturing, such as silicon, face limitations at smaller scales. New materials like high-k dielectrics and metal gates have been introduced, but they also come with their own set of challenges.
6. **Manufacturing Complexity and Costs**: The fabrication process for smaller transistors is increasingly complex and costly. The precision required for manufacturing at nanoscale dimensions makes it difficult to maintain high yields and affordability.
7. **Voltage Scaling Issues**: While transistor dimensions have continued to shrink, the voltage required to operate these transistors has not scaled down proportionally. Higher electric fields can lead to increased wear and reduced reliability.

Due to these challenges, the industry has been exploring alternative approaches to continue improving computing performance. These include new architectures (such as multi-core processors), **three-dimensional (3D) stacking of chips**, specialized accelerators (like GPUs), and new computing paradigms (such as quantum computing and neuromorphic computing).

Foundry 1.0

- Current semiconductor business has been focused on driving smaller transistors.
  - High development cost
  - High capital cost
  - Long development times
  - Expensive design tools
  - High risk

- Twilight of Moore's Law

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A New Semiconductor Industry Paradigm

Foundry 2.0 –

A Finishing Foundry that takes the standardized building blocks from traditional semiconductor manufacturers and uses advanced packaging and additive manufacturing to create highly customized components with superior performance targeting small and medium sized markets.

Foundry 2.0 Opportunity

- There are no de facto winners
  - Intel, AMD, Xilinx, Marvell, -- Currently IDM driven but nascent
- Low capital costs
  - More than an order of magnitude lower capital costs
- Supports low and medium volume flows – High mix fabrication
  - USG, startups, large swath of industry
    - More cost effective
  - Competition is FPGAs 10x to 50x lower component cost
- IP centric Knowledge based value
- Phased approach works well
- Complementary to Foundry 1.0
  - Partnering Customers, Capital, Pile-on

Changing to a High-Mix, Lower Volume Manufacturing Model

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Why the Change in Direction?

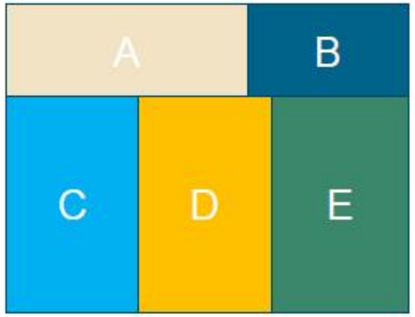
- Transistor cost is increasing
  - To reduce cost, we need to sell the consumer fewer transistors
  - Most semiconductor devices have the kitchen sink
  - NRE is high so we can't target markets
- Chiplets offer reuse – effectively $0 NRE
- Advanced packaging NREs run ~100x less cost than leading edge node NREs
- Chiplet to chiplet power and delay is competitive with on die
- Chiplets can target markets – use only necessary transistors

→ Low NRE → Niche Market → Fewer Transistors → Lower Cost Composite Device

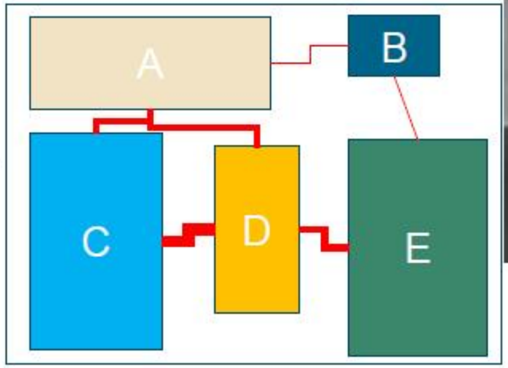
Moore's Law for the Next Generation

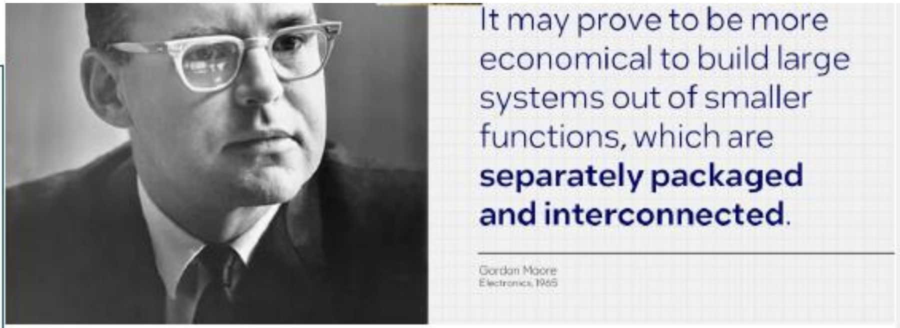
Drivers for Chiplet Integration

SOC

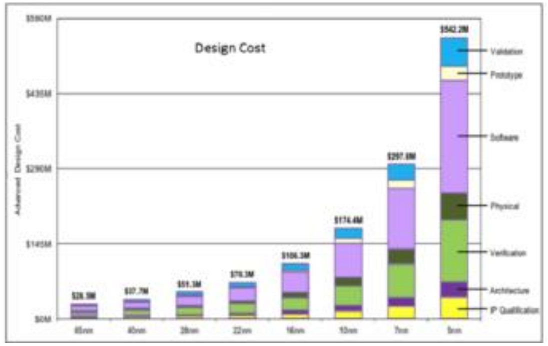


Shared Package





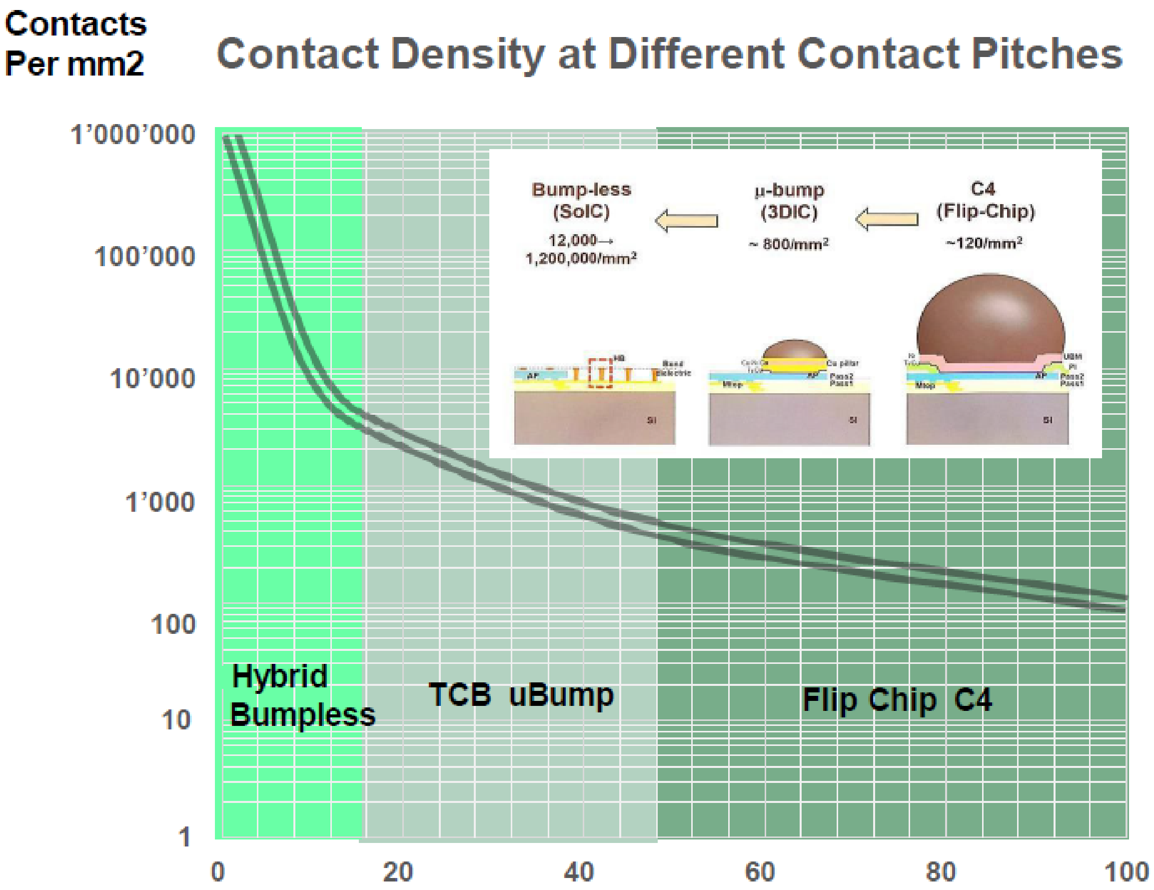
- Difficult
- Very Costly
- Low Initial Die Yield



Pros
- **SWAP**
- Flexibility
- Optimized Performance
- Lower Power
- Shorten Time-to-Market
- Gordon Moore predicted that eventually one would go to packaging individual chips – Original paper.
- Thermal optimization
- Spin multiple products faster

Cons
- **Create System Integration Ecosystem (Supply Chain and Business).**
- KGD – Known Good Die
- Establish a pull by customers
- Standards
- Software Design Tools
- Yield Loss Ownership

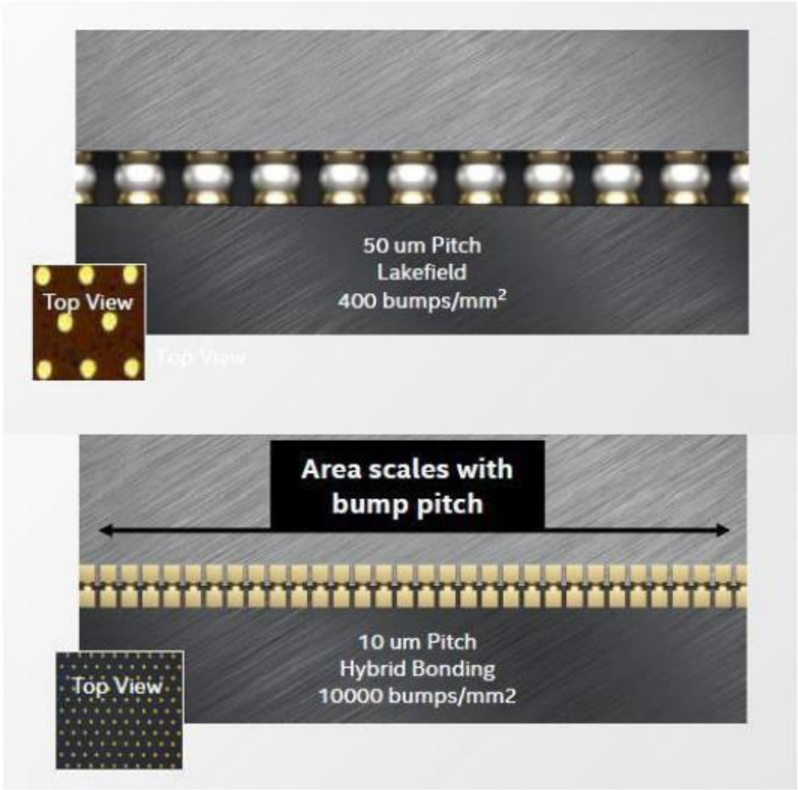
Hybrid Bonding Innovation



Drive to 1um pitch I/O

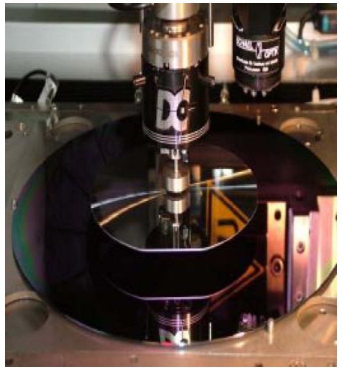
Tom Strothman, BESI

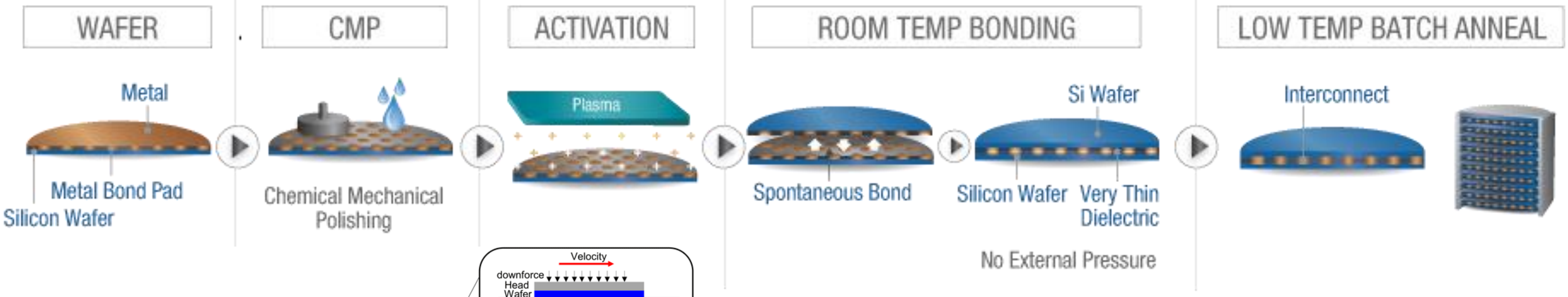
More Contacts Enable More Data



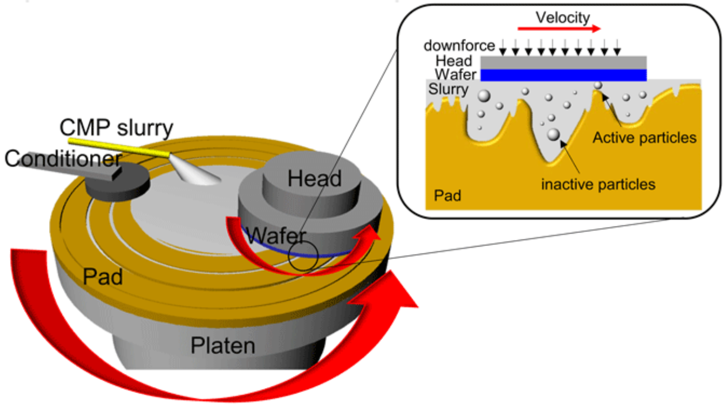
Intel

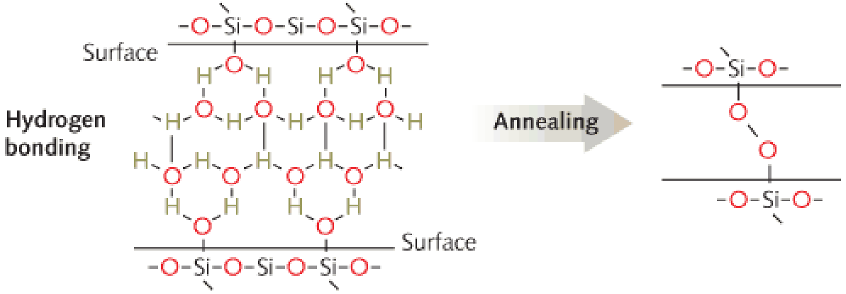
DBI®: Low Temperature Hybrid Bonding Process



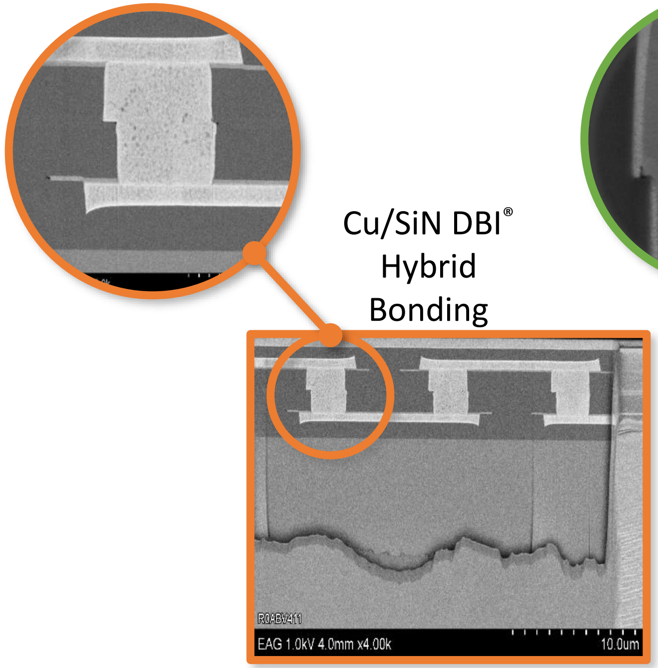


Jihoon Seo / Materials Research Society



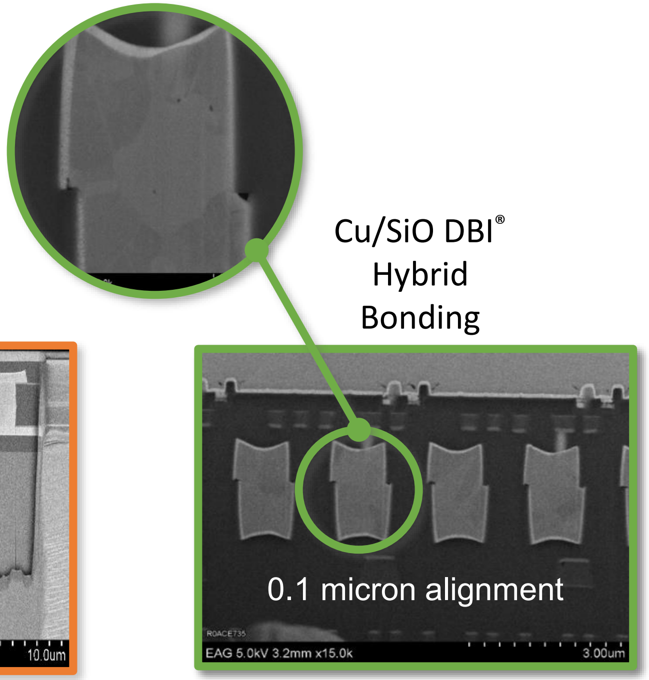


Hybrid Bonding Interconnect Pitch Scaling



Cu/SiN DBI®
Hybrid
Bonding

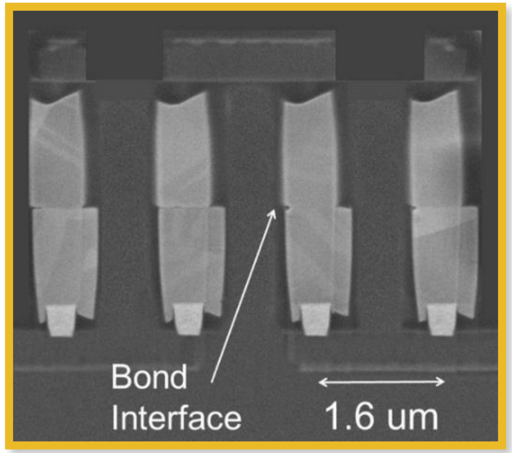
10 μm DBI® pitch, 300℃



Cu/SiO DBI®
Hybrid
Bonding

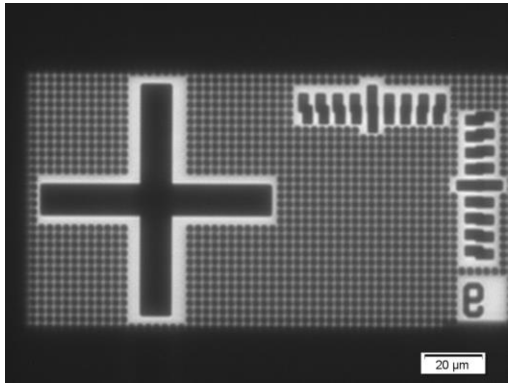
1.9 μm DBI® pitch, 300℃

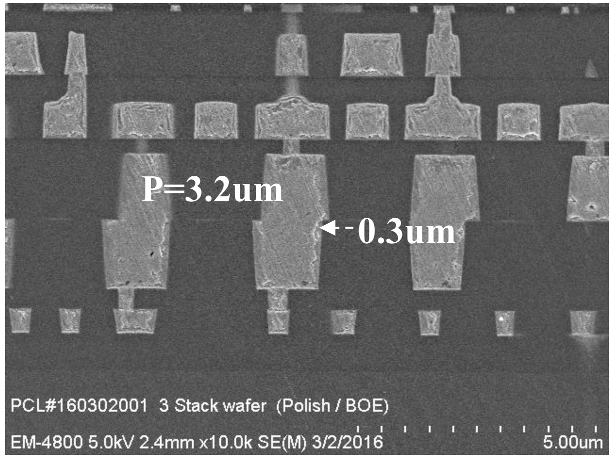
Scalable To < 1um Pitch
0.8um Pitch Demonstrated



1.6 μm DBI® pitch, 300℃

- WtoW 3sigma < ±1um misalign performance
- DtoW 3sigma < ±200nm misalign performance
- Production Minimum pitch = 2.44um
- Best alignment is achieved with face-to-face bonding





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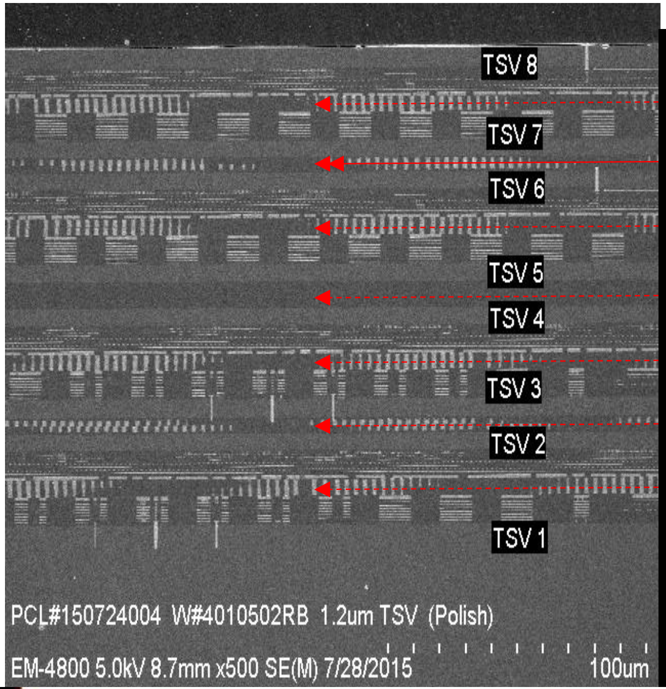
Advanced Packaging: Bonding

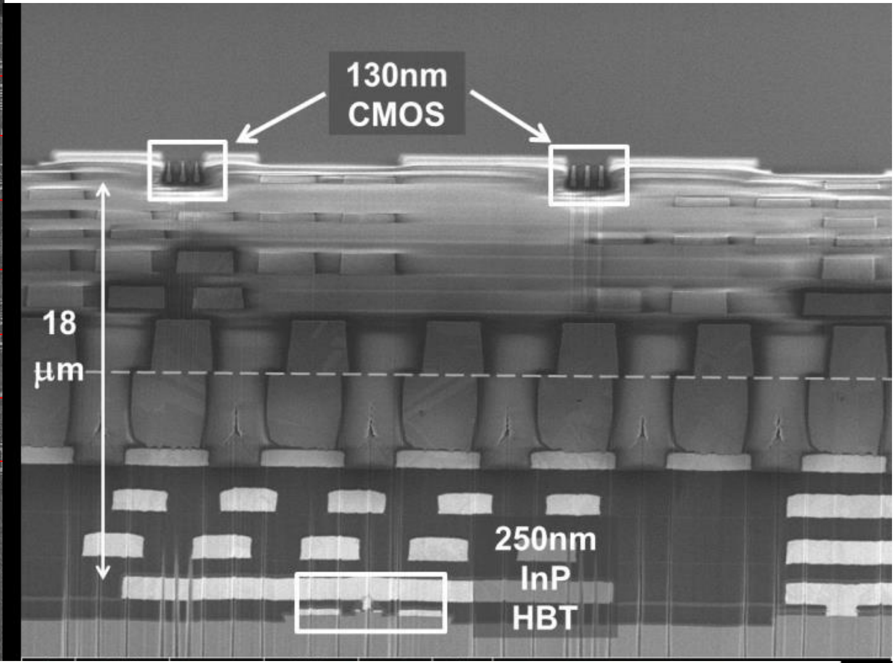
Millimeters ⇨ Microns

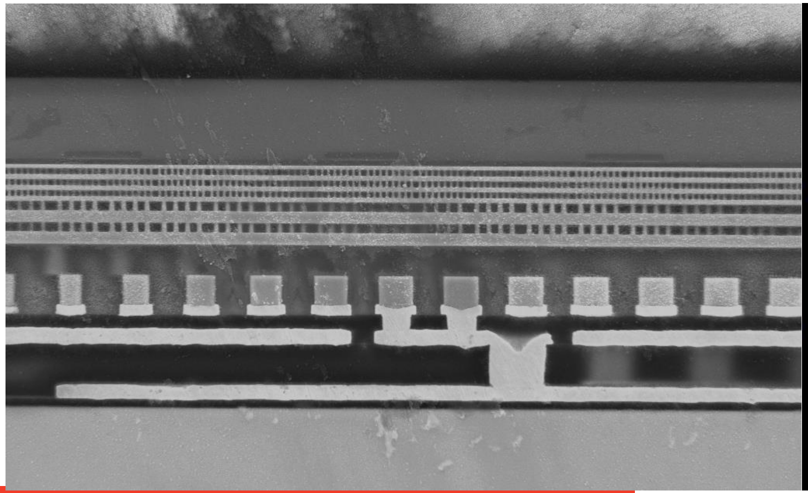
Kilograms ⇨ Grams

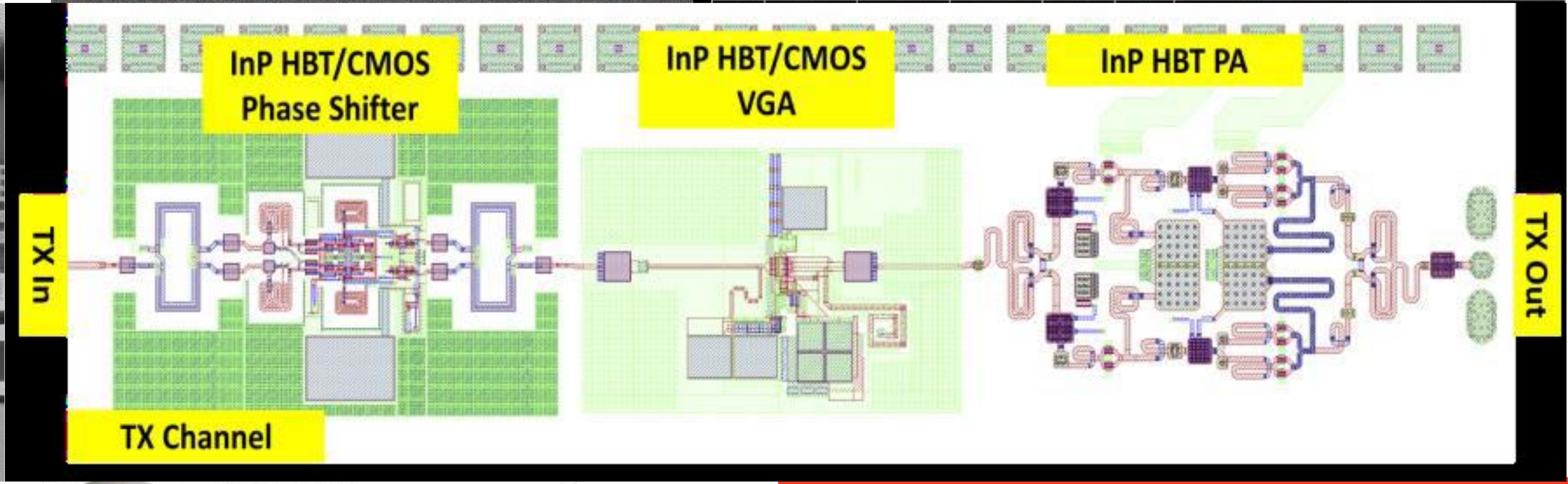
Mixed Materials

Best of Class









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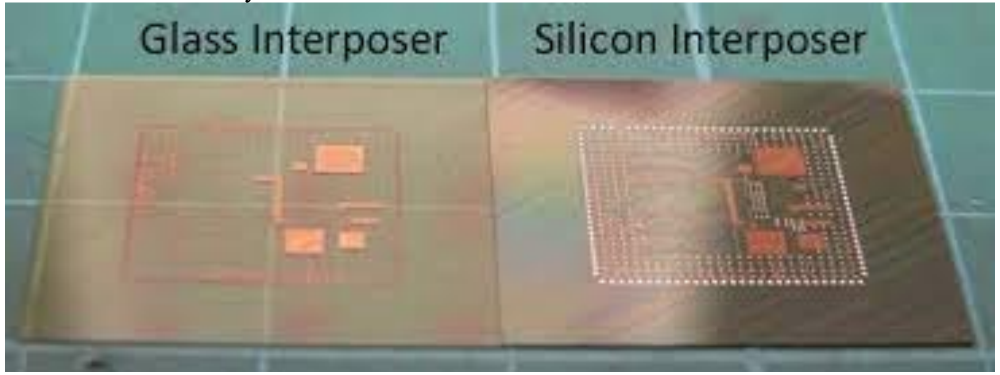
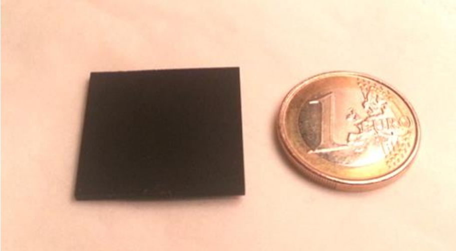
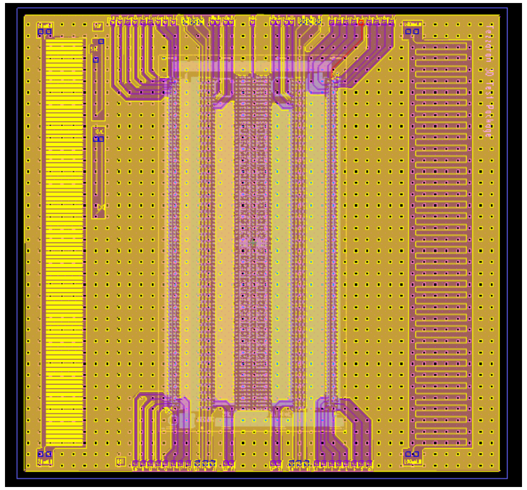
Advanced Packaging: Interposers

- ➢Bigger, Better, Faster
- ➢Lower Power

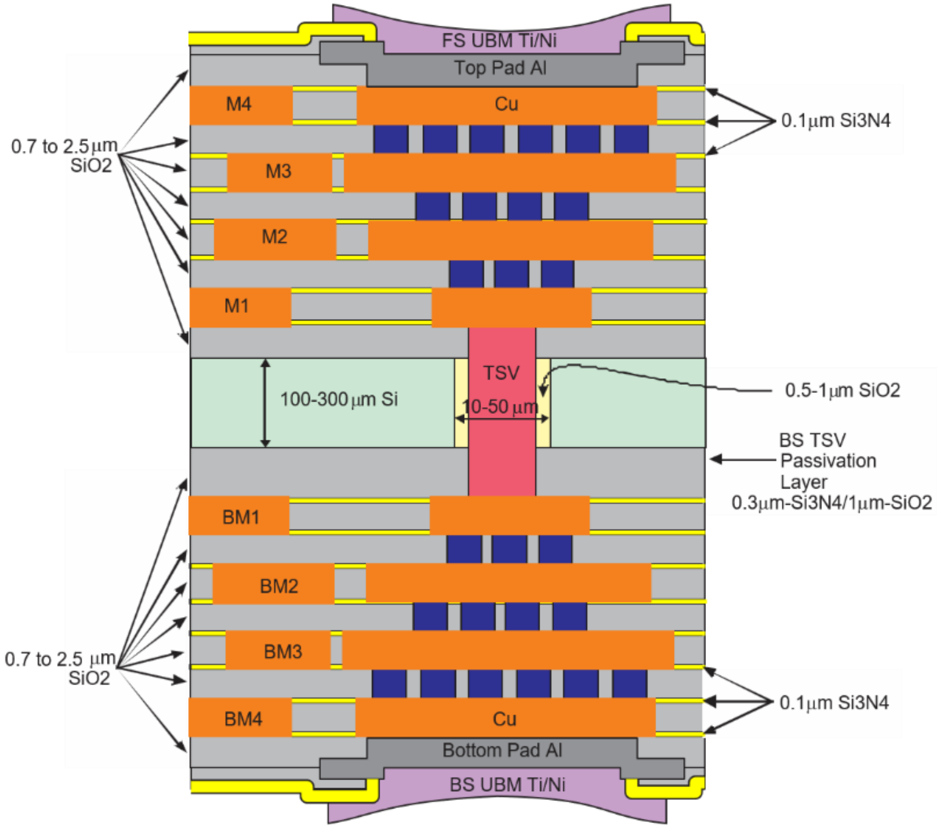
Mosaic Microsystems

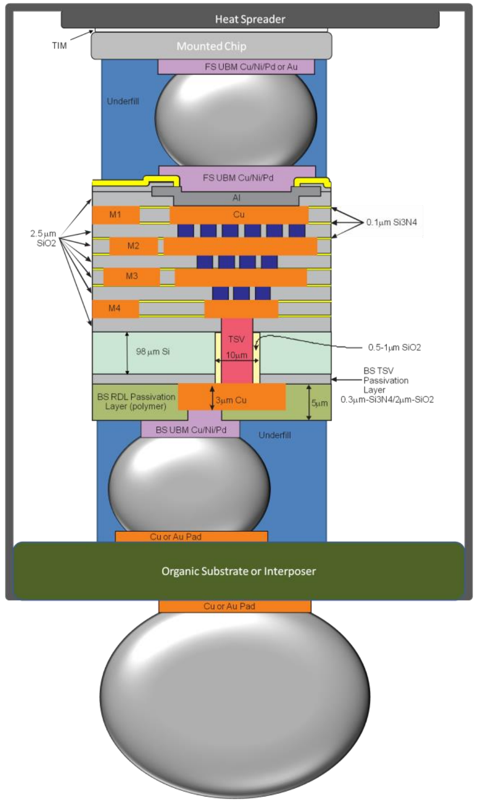






Up to 8 layers of wiring available





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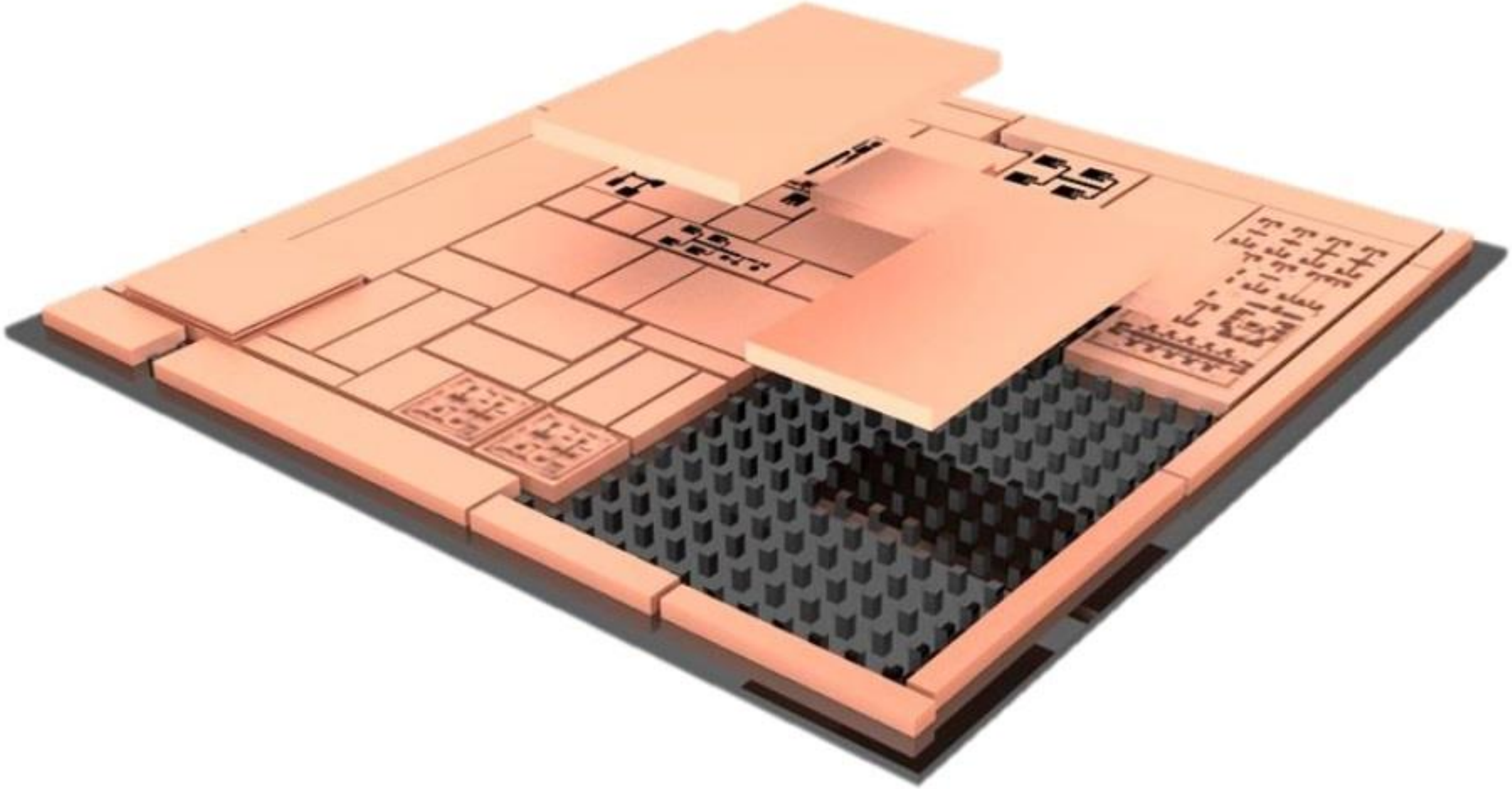
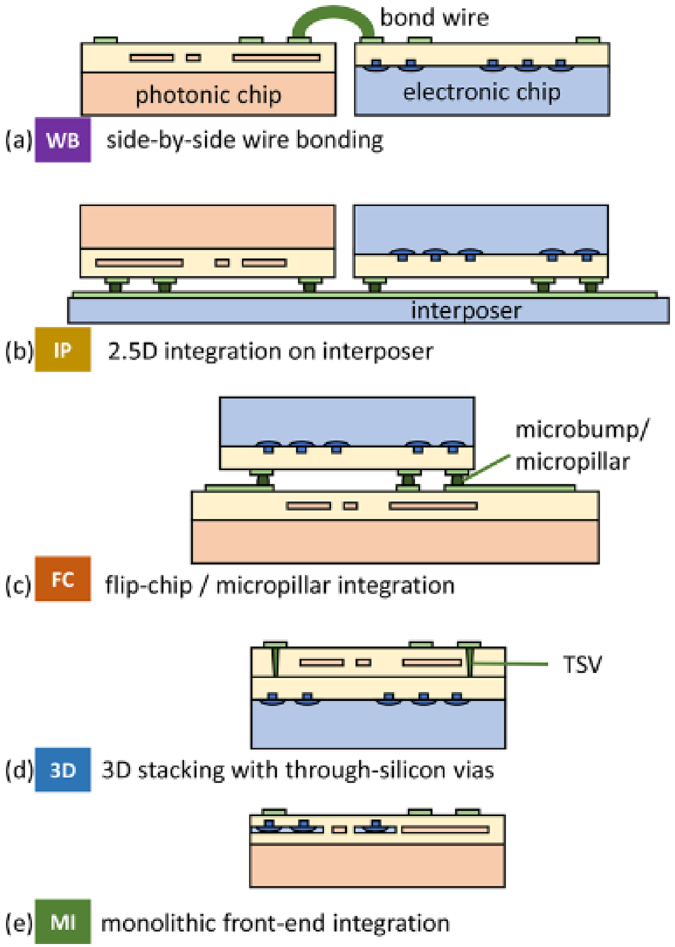
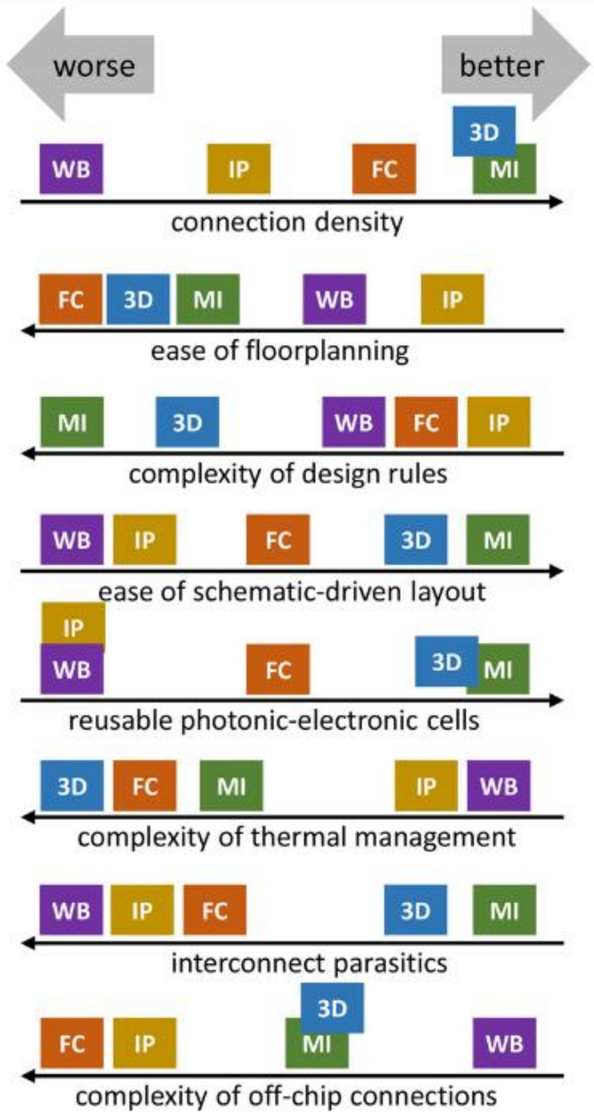
The Promise of Chiplets … Just Like Legos®



Approaches for Integration of Photonics and Electronics



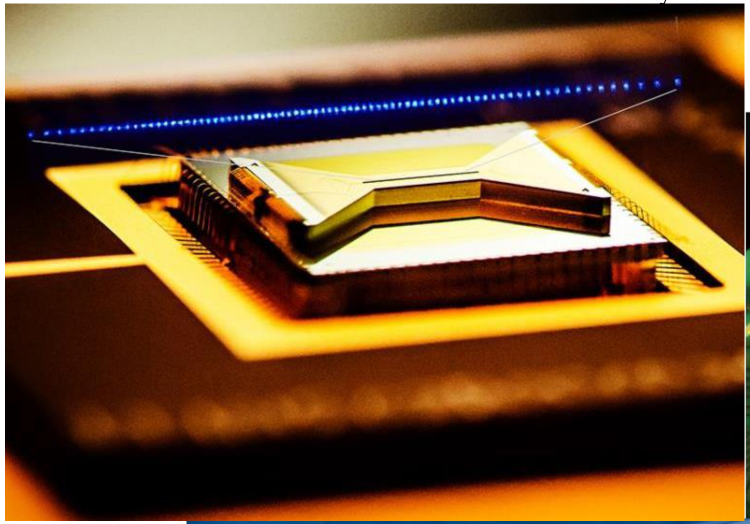


W Bogaerts L. Chrostowski – Laser Photonics Rev. 2018, 12

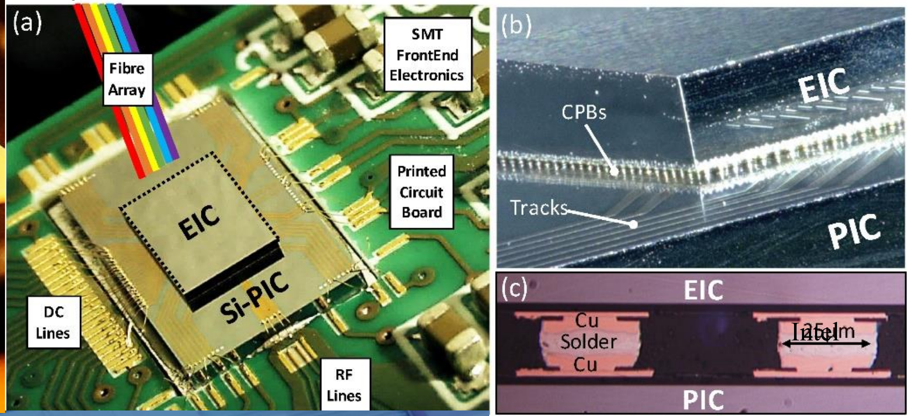
AP Drivers: Photonics & Quantum

- I/O
  - Tb/s, <<100fJ/b
    - SiP 500ff I/O Load
    - 2.5D 25ff I/O Load
    - 3D 3ff I/O Load
- Processing
  - "Quantum Leaps"

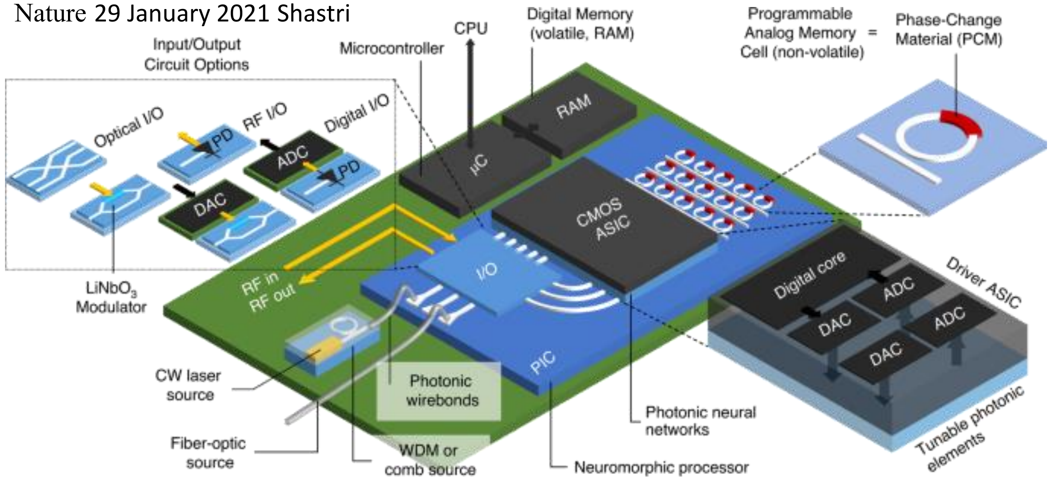
Honeywell

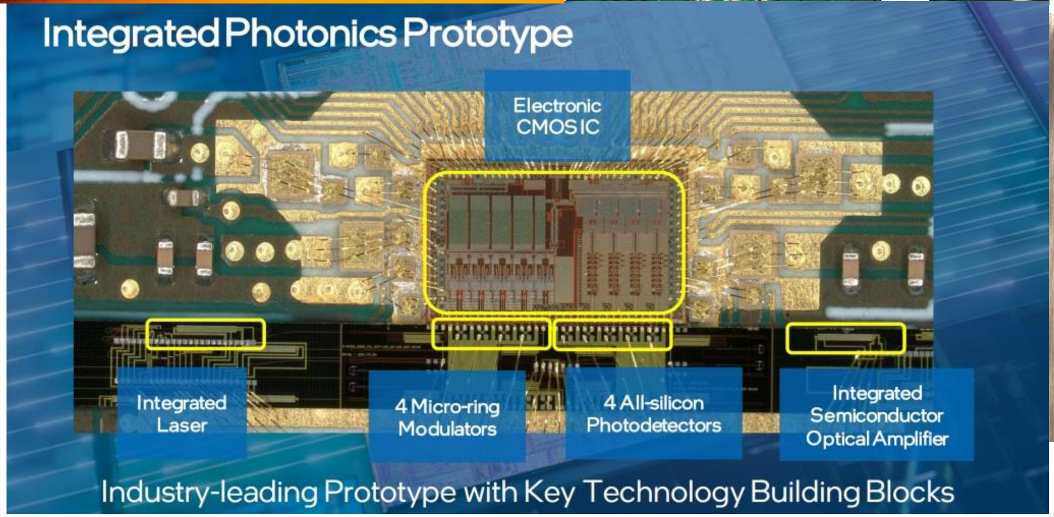


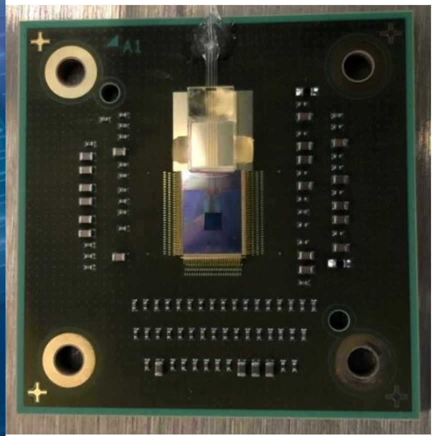
Tyndall National Institute Carroll et al



Nature 29 January 2021 Shastri







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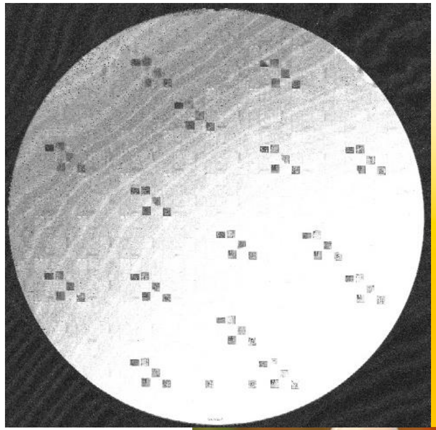
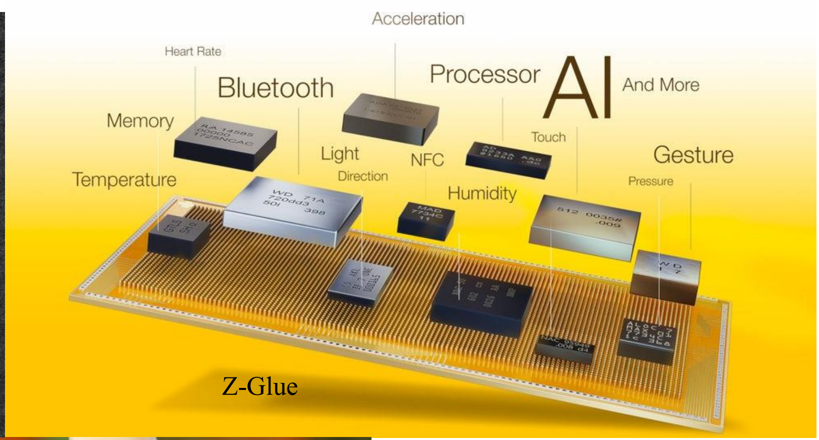
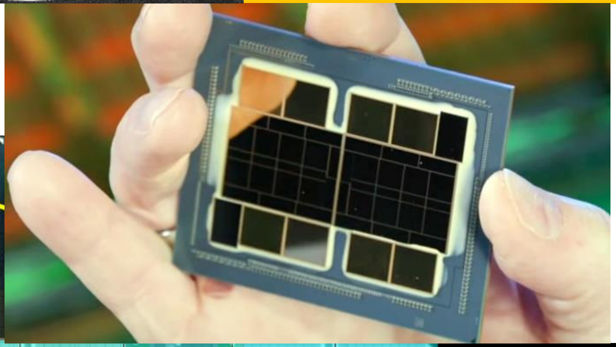
Advanced Packaging: Chiplets

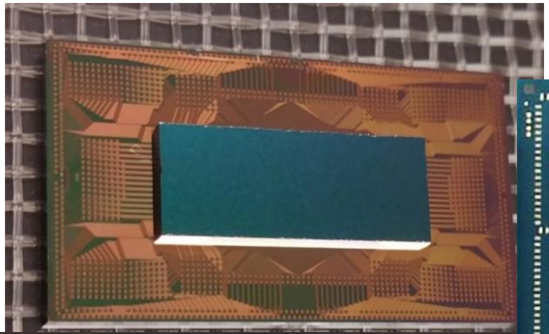
- Provides:
  - Best of Class Everything
  - Easy retargeting
  - Lower risk
  - IP reuse
  - Lower cost

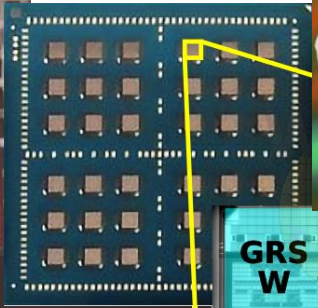




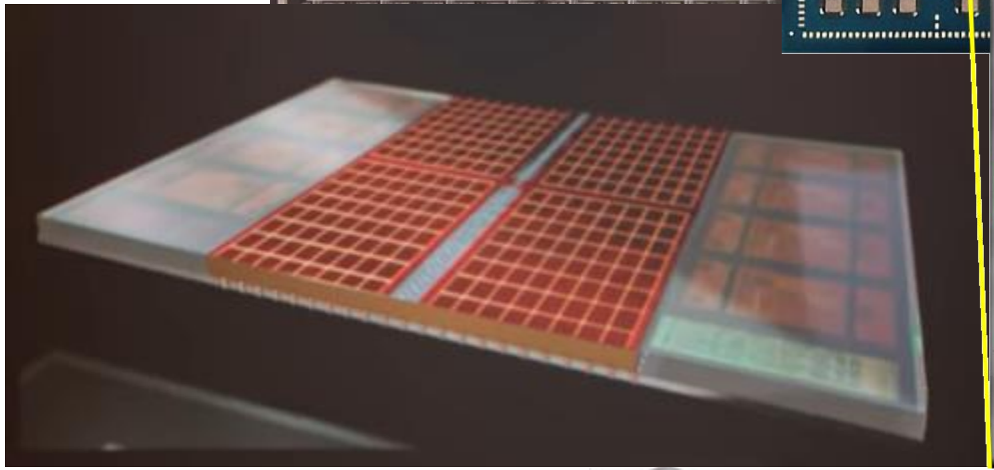
Z-Glue

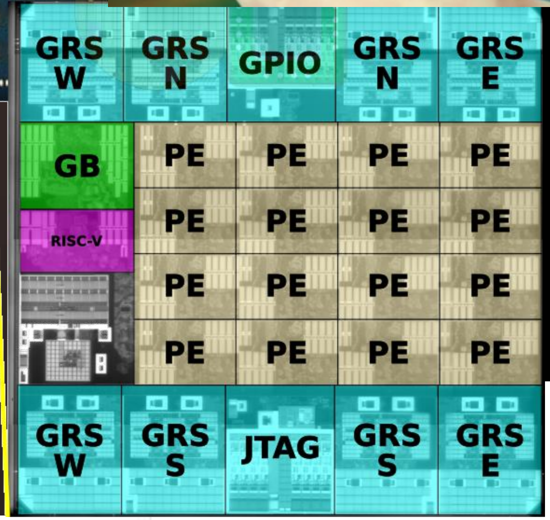

Intel





AMD





Intel

nVidia

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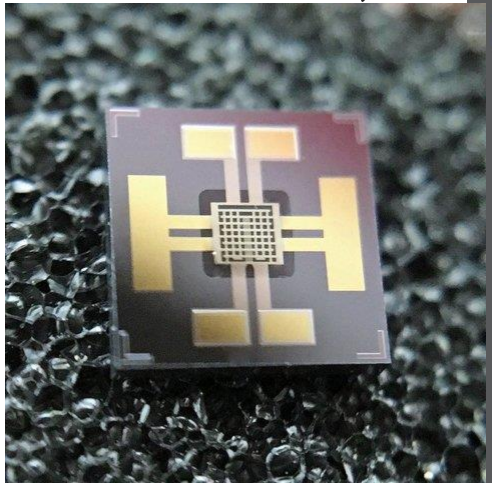
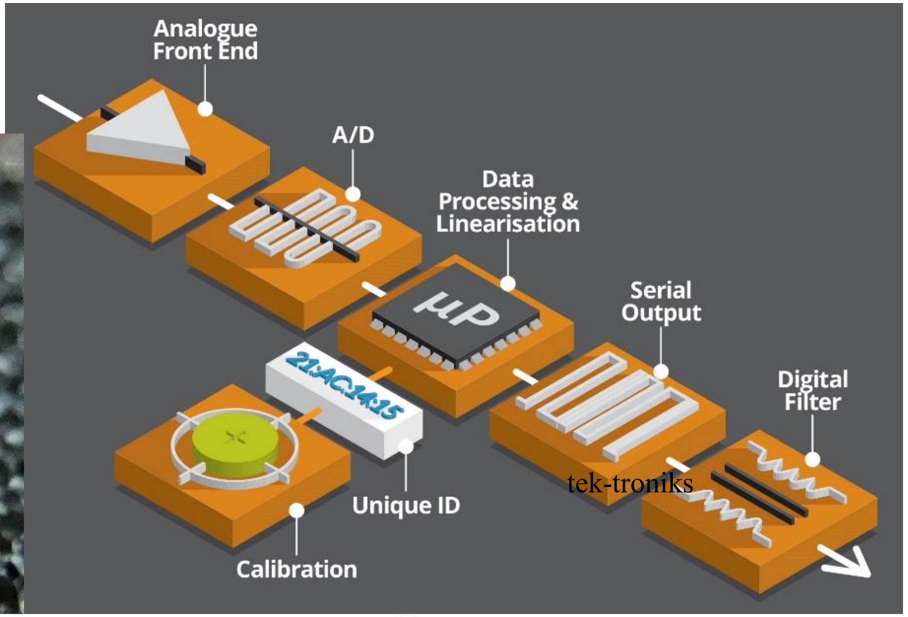
AP Drivers: Intelligent Sensors and Edge Compute

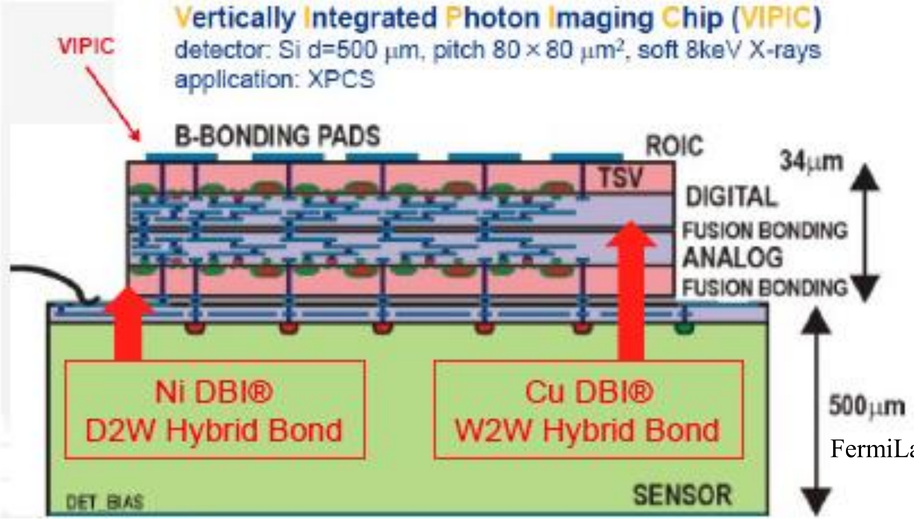
- Communication is limited
  - Data movement costs power
  - Data movement costs time
  - Data movement costs money
  - You can't aways "phone-home"

Micralyne

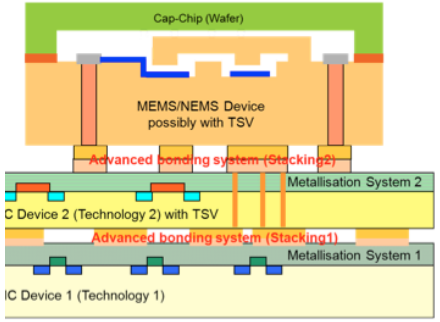




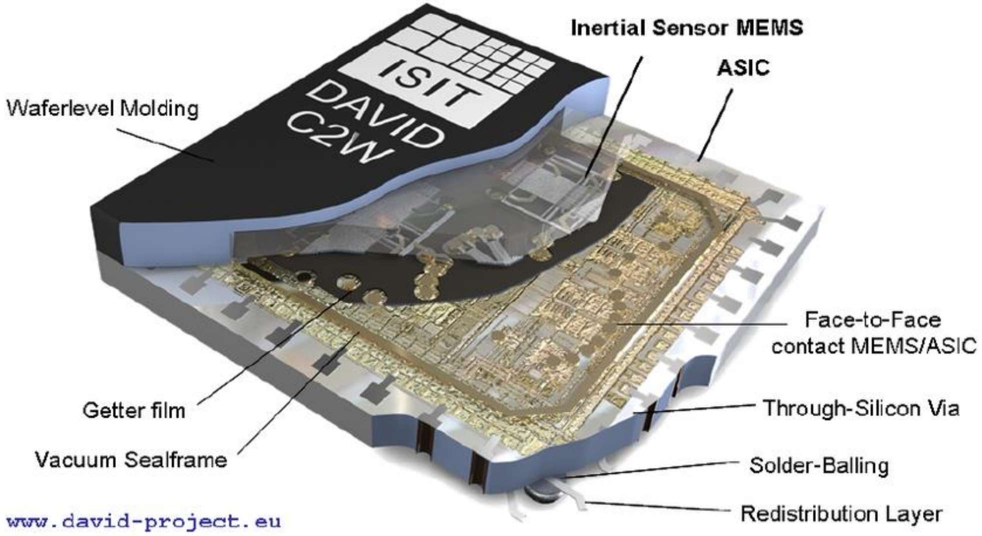
tek-troniks



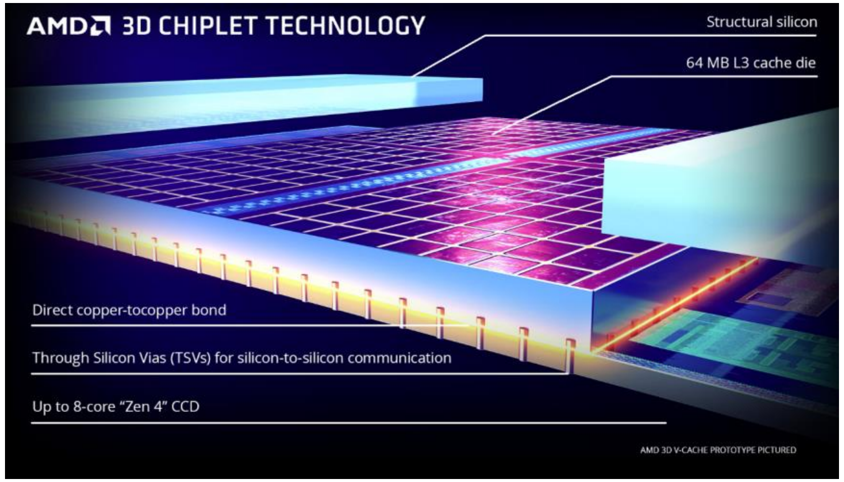
FermiLab

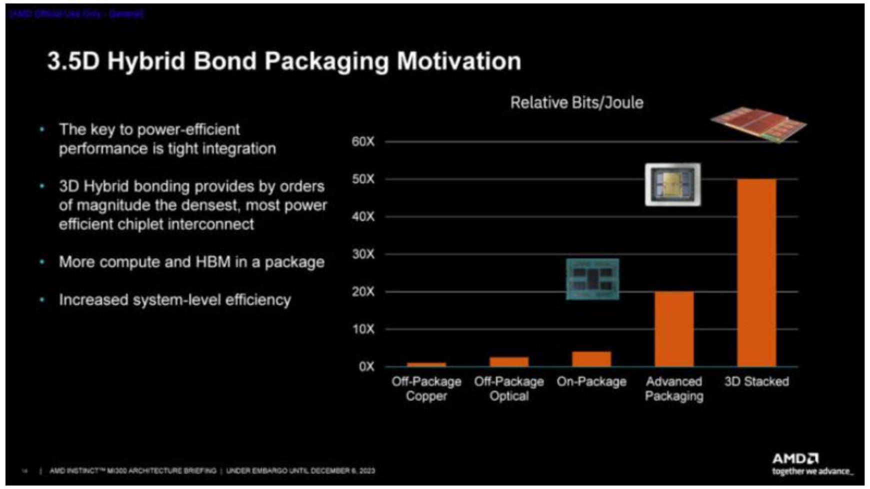


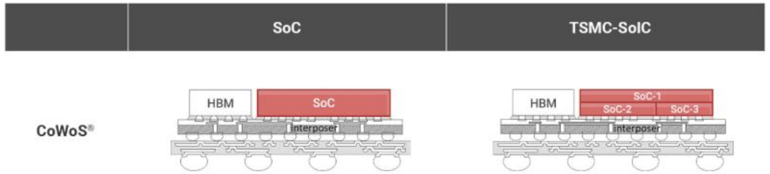
3DinCites



Hybrid Bonding is Enabling the Next Generation of Packages







Samsung maintains hybrid bonding needed for HBM 16H

Noh Tae Min 기자 | 승인 2024.06.11 09:02 | 댓글 0

Unlike SK Hynix will continue MR-MUF in 16-stack HBM

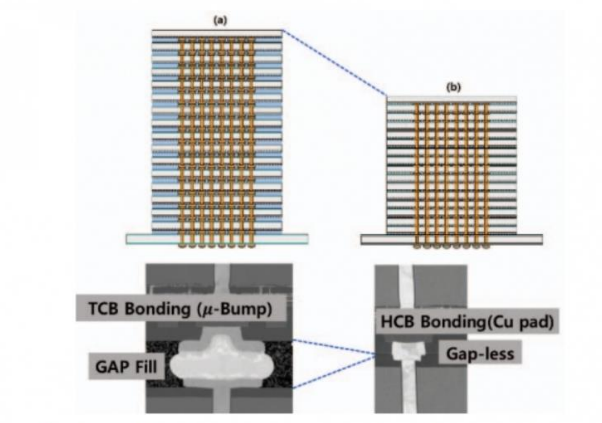


Fig. 1 16H HBM structure diagram and vertical structure of joint gap; (a) Conventional TCB Bonding (b) HCB Bonding

Samsung is also working to develop a bump-less package by 2025. The package is aimed at high-layer HBM and can help lower the height of the packages. The technology is also called Cu to Cu, direct bonding or hybrid bonding.

출처 : THE ELEC, Korea Electronics Industry Media(http://thelec.net)

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A Change In Perspective Foundry 2.0

- A new focus on next generation semiconductors created by
  - Advanced Packaging
  - Additive Semiconductor Manufacturing
  - True heterogenous integration
  - Interconnect focused – all BEoL additive
    - Better ROI
    - Lower development costs
    - Lower CAPEX
  - Leveraging existing foundries
    - Split Fab
  - More Than Moore Technologies
    - IP Centric
    - IP driven value – not cost of capital

System Level Moore's Law

Split Rock Lens – StackExchange

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Thank You

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