A Global View Versus a U.S. Focus on Outsourced Assembly and Test (OSAT) Facilities to Support Wafer Level Packaging

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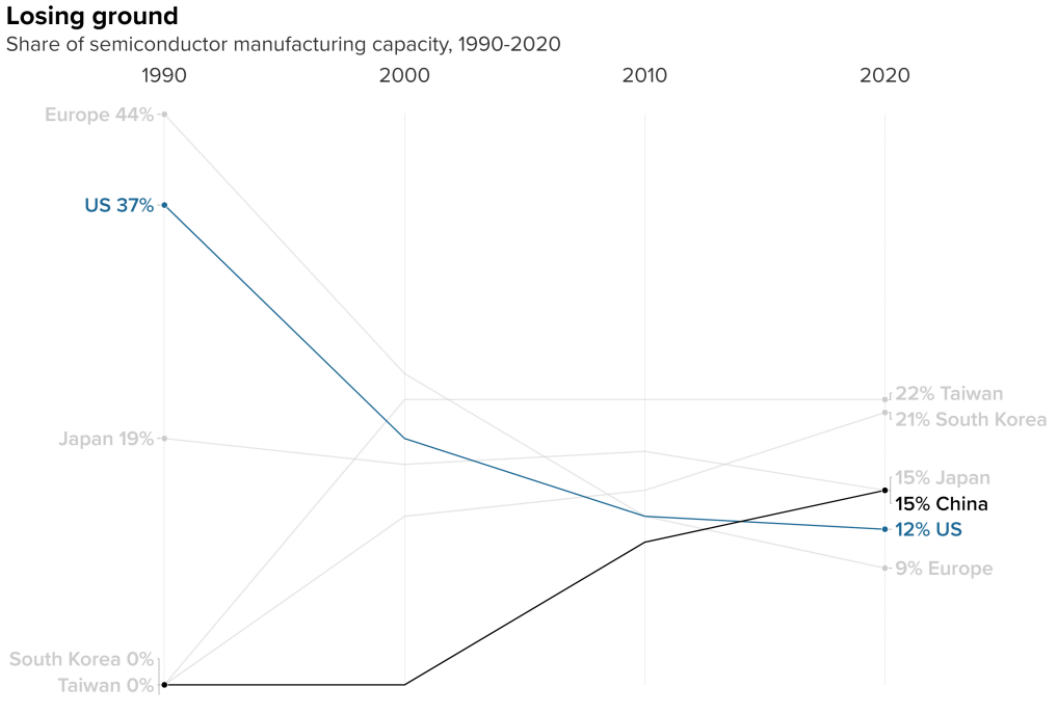
18 pages

Outline/Agenda

- Introduction
- Current Landscape
- Emerging Paradigm
- Collaboration with IDMs and Fabless Companies
- Strategic Path Forward for the U.S.
- Summary

Semiconductor Mfg. Capacity



Source: Semiconductor Industry Association/BCG.

Global Landscape

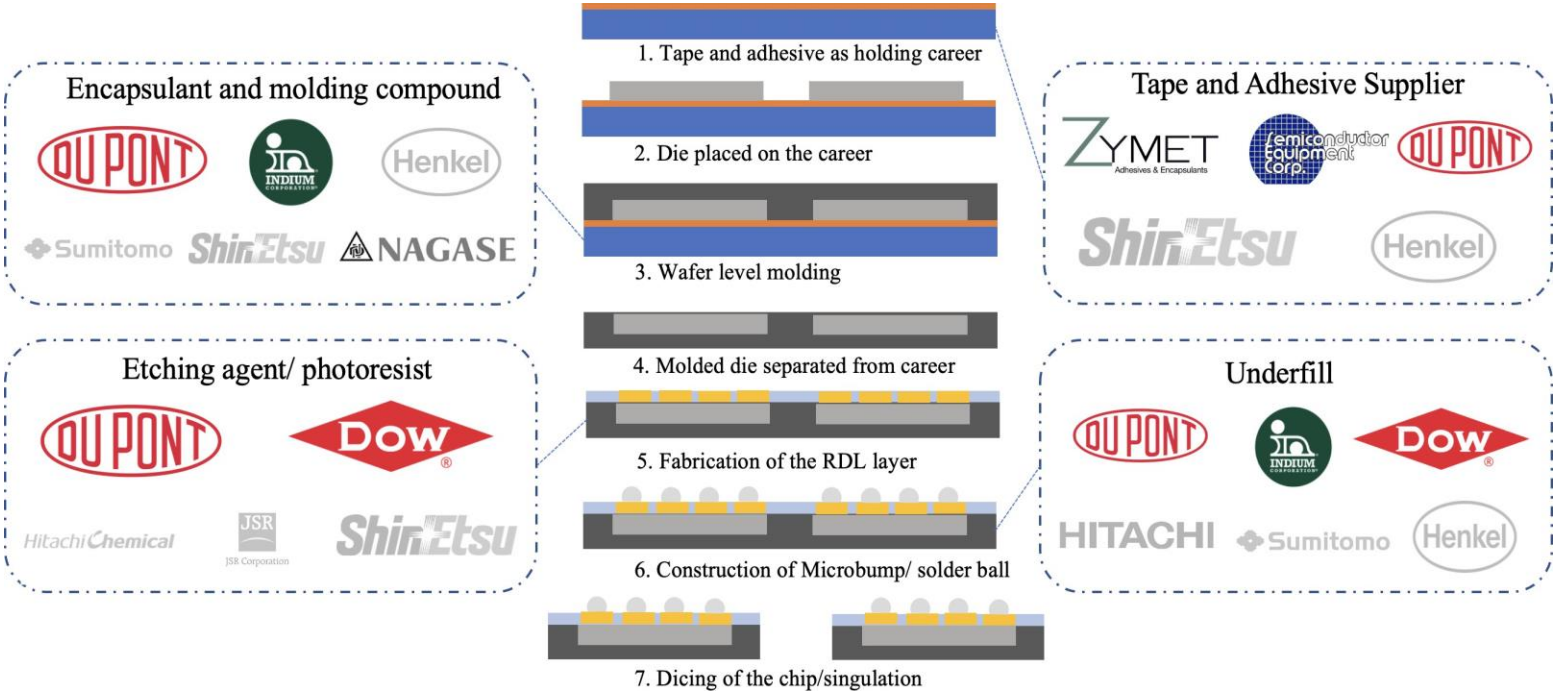
Reference: Yole 2023

North America is in a Weak Position for AP/HI

Current Landscape

- Globally, semiconductor giants in Asia have established dominance in OSAT-driven innovations.
- These advancements have allowed these nations to maintain leadership in heterogeneous integration and modular semiconductor designs.
- In contrast, the United States faces unique challenges, including fragmented supply chains, limited domestic infrastructure, and the lack of coordinated strategies for integrating advanced WLP into its semiconductor ecosystem

Current Landscape

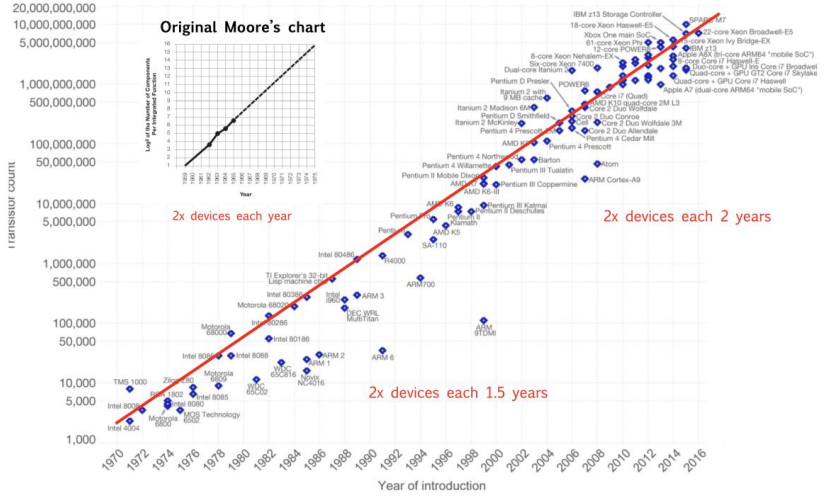


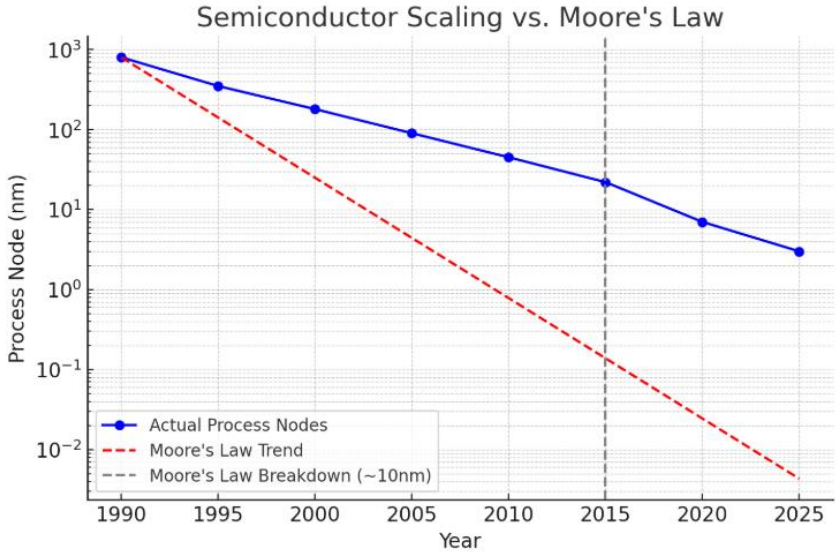
. Onshore and Offshore (grey-colored) suppliers of WLP in the U.S.

Current Landscape

- By providing actionable insights, this presentation outlines a roadmap for U.S. OSAT facilities to close the gap with global leaders.
- The roadmap for the U.S. emphasizes ecosystem collaboration with Integrated Device Manufacturers (IDMs), fabless companies, and academia to align innovations with industry requirements.
- The semiconductor industry is undergoing a profound transformation, transitioning from the rigid Foundry 1.0 model to the dynamic, collaborative framework of Foundry 2.0.

Moore’s Law





Moore’s Law states that the number of transistors in a chip roughly doubles every two years, whereas its cost if halved over the same timeframe. This trend started to break down around the 10nm to 7nm nodes.

The data in the graph is based on historical semiconductor process nodes from leading manufacturers like **Intel, TSMC, and Samsung**, along with the general trend of Moore’s Law. While it's an approximation, it aligns with industry scaling trends observed over the past few decades.

Moore’s Second Law

Moore's Second Law, sometimes called **"Rock's Law"**, states that:

"The cost of a semiconductor fab doubles roughly every four years."

Key Implications:

1. **Escalating Fab Costs** – Modern semiconductor fabs now cost **tens of billions of dollars** (e.g., TSMC’s 3nm fab costs over **$20 billion**).
2. **Consolidation of the Industry** – Fewer companies can afford to develop cutting-edge nodes, leading to **TSMC, Intel, and Samsung dominating the field**.
3. **Shift to Chiplet Architectures** – Instead of monolithic chips, companies are increasingly using **chiplets and advanced packaging** to manage costs and complexity.

Moore’s Second Law is one of the reasons why Moore’s First Law (transistor scaling) has slowed—economic feasibility has become a major limiting factor.

Effective End of Moore's Law

Moore's Law was first and foremost a statement about economics. We could shrink transistors and build more of them for about the same cost.

- This has been the basic premise of the semiconductor industry for 50 years and was true up until the last few years.
- Today we can indeed shrink transistors further, but the cost per transistor no longer declines.
  - We can get something a little more compact
  - Perhaps a little less power
  - But we pay more for these features now.

Breakdown of Dennard Scaling

Dennard scaling, the principle that transistor power density remains constant as transistors get smaller, has been a fundamental driver of improvements in computing performance for decades. However, this scaling has slowed down significantly in recent years due to several technical and physical challenges:

1. **Leakage Current**: As transistors shrink, the thickness of the gate oxide layer decreases, leading to increased leakage currents. This leakage contributes to higher power consumption and heat generation, negating the benefits of smaller transistor sizes.
2. **Short Channel Effects**: When transistors become extremely small, short channel effects such as drain-induced barrier lowering (DIBL) and threshold voltage roll-off become more pronounced. These effects degrade the performance and reliability of the transistors.
3. **Heat Dissipation**: As transistors shrink and their density increases, the ability to effectively dissipate heat becomes a critical issue. The heat generated by densely packed transistors can lead to thermal management challenges, impacting performance and longevity.
4. **Quantum Effects**: At very small scales, quantum mechanical effects become significant. Quantum tunneling, for instance, can cause electrons to pass through insulating barriers, leading to increased power consumption and unpredictable behavior.
5. **Material Limitations**: The traditional materials used in semiconductor manufacturing, such as silicon, face limitations at smaller scales. New materials like high-k dielectrics and metal gates have been introduced, but they also come with their own set of challenges.
6. **Manufacturing Complexity and Costs**: The fabrication process for smaller transistors is increasingly complex and costly. The precision required for manufacturing at nanoscale dimensions makes it difficult to maintain high yields and affordability.
7. **Voltage Scaling Issues**: While transistor dimensions have continued to shrink, the voltage required to operate these transistors has not scaled down proportionally. Higher electric fields can lead to increased wear and reduced reliability.

Due to these challenges, the industry has been exploring alternative approaches to continue improving computing performance. These include new architectures (such as multi-core processors), **three-dimensional (3D) stacking of chips**, specialized accelerators (like GPUs), and new computing paradigms (such as quantum computing and neuromorphic computing).

Foundry 1.0

Current semiconductor business has been focused on driving smaller transistors.

- High development cost
- High capital cost
- Long development times
- Expensive design tools
- High risk

Twilight of Moore's Law

TSMC SOTA Fab in Arizona

Limitations of the Current Foundry 1.0 Approach

- The Foundry 1.0 model epitomizes the traditional low-mix, high-volume (LMHV) approach to semiconductor manufacturing, prioritizing transistor scaling for mass production.
- Globally, LMHV practices thrived in countries with robust resources and established semiconductor ecosystems, like countries in Asia, where massive investments bolstered competitive scaling.
- Foundry 1.0 excelled at scaling for general-purpose chips but lacked the agility required to adapt quickly to emerging demands.
- This rigidity was exacerbated by the “kitchen sink” approach, which included monolithic chip designs packed with excessive functionalities to suit broader markets.

A New Semiconductor Industry Paradigm

Foundry 2.0 –

A Finishing Foundry that takes the standardized building blocks from traditional semiconductor manufacturers and uses advanced packaging and additive manufacturing to create highly customized components with superior performance targeting small and medium sized markets.

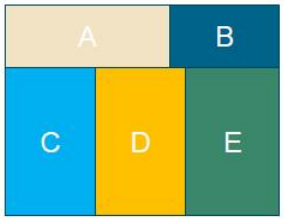
Introduction to Foundry 2.0

- Foundry 2.0 embraces the agility and customization of high-mix low-volume (HMLV) strategies.
- At its core, Foundry 2.0 fosters collaboration, breaking down silos to create an interconnected ecosystem that brings designers, manufacturers, and OSAT facilities into closer alignment.
- This collaborative framework makes Foundry 2.0 uniquely capable of addressing rapidly evolving technological needs, particularly in markets that prioritize performance, efficiency, and compact design.
- **For the U.S., Foundry 2.0 represents a strategic opportunity to regain semiconductor leadership.**

Technology Drivers for Chiplets

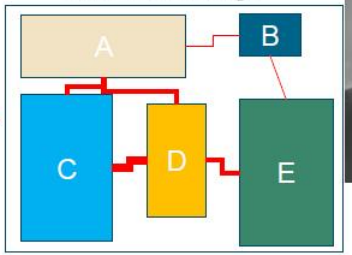
Drivers for Chiplet Integration

SOC



End of Cost Advantage of Moore's Law

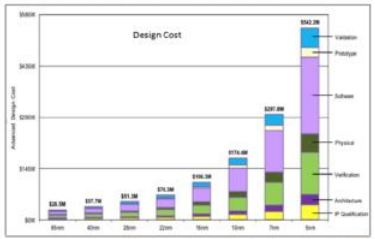
Shared Package



It may prove to be more economical to build large systems out of smaller functions, which are **separately packaged and interconnected.**

Gordon Moore
Electronics, 1965

- Difficult
- Very Costly
- Low Initial Die Yield



Moore's Law is Dead – Long-live the Chiplet!

Pros

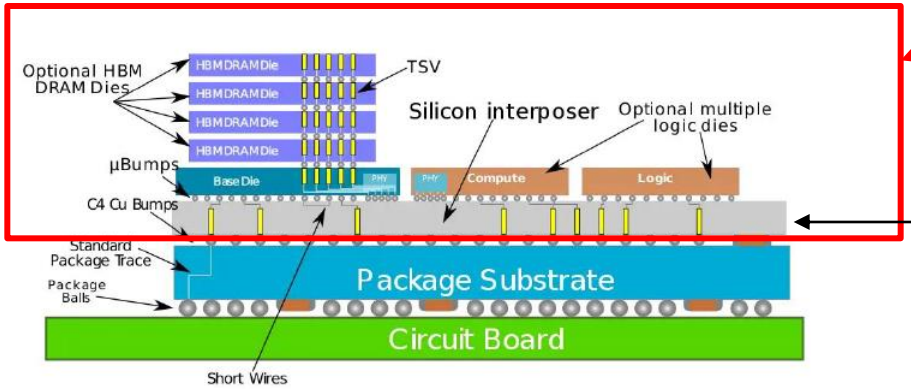
- **SWAP**
- Flexibility
- Optimized Performance
- Lower Power
- Shorten Time-to-Market
- Gordon Moore predicted that eventually one would go to packaging individual chips – Original paper.
- Thermal optimization
- Spin multiple products faster

Cons

- **Create System Integration Ecosystem (Supply Chain and Business).**
- KGD – Known Good Die
- Establish a pull by customers
- Standards
- Software Design Tools
- Yield Loss Ownership

What is Heterogeneous Integration?

Advanced Packaging



Heterogeneous Integration – Integration of Chiplets 2.5D and 3D

Si-Interposer

Foundry 2.0 Opportunity

There are no de facto winners

- Intel, AMD, Xilinx, Marvell, -- Currently IDM driven but nascent

Low capital costs

- More than an order of magnitude lower capital costs

Supports low and medium volume flows – HMLV fabrication model

- USG, startups, large swath of industry
  - More cost effective
- Competition is FPGAs 10x to 50x lower component cost

IP centric Knowledge based value

Phased approach works well

Complementary to Foundry 1.0

- Partnering Customers, Capital, Pile-on

Changing to a High-Mix, Lower Volume Manufacturing Model

Why the Change in Direction?

Transistor cost is increasing
- To reduce cost, we need to sell the consumer fewer transistors
- Most semiconductor devices have the kitchen sink
- NRE is high so we can't target markets

Chiplets offer reuse – effectively $0 NRE

Advanced packaging NREs run ~100x less cost than leading edge node NREs

Chiplet to chiplet power and delay is competitive with on die

Chiplets can target markets – use only necessary transistors

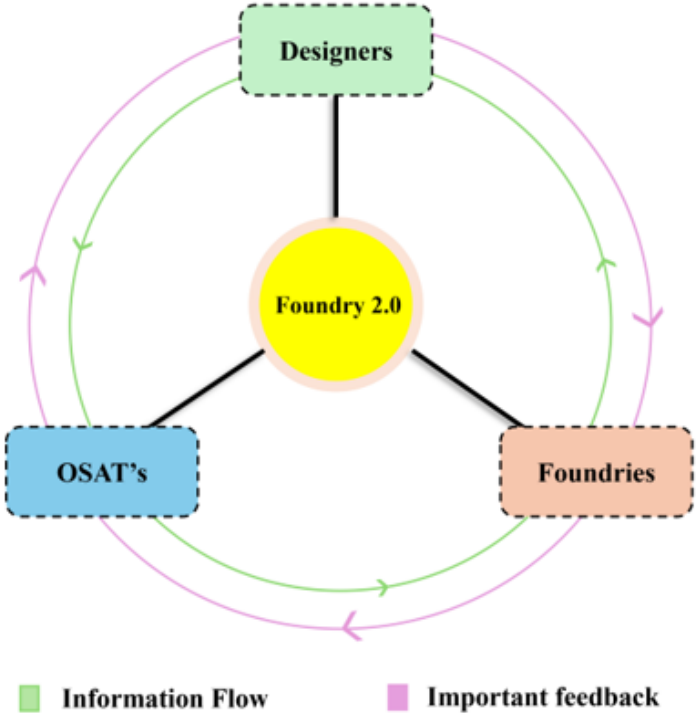
→ Low NRE → Niche Market → Fewer Transistors → Lower Cost Composite Device

Moore's Law for the Next Generation

Comparison of Two Models

Aspect	Foundry 1.0	Foundry 2.0
Production Model	Low-Mix High Volume	High-Mix Low Volume
Key Features	Pure-play fabrication services	Design support, heterogeneous integration, and innovation
Packaging	Monolithic chips	Chiplet-based architectures, 2.5D/3D integration
Market Strategy	Low Mix, High Volume: Mass production of standardized chips for broad applications.	High Mix, Low Volume: Production of customized, application-specific chips for niche and emerging markets.
Collaboration Model	Isolated operations, minimal designer-foundry inter-action	Ecosystem-driven real-time collaboration across stakeholders
Government Support	Limited support; industry-driven	Backed by government initiatives across the world and CHIPS Act in the U.S.
Flexibility	Low, focused on broad markets	High, with adaptability for emerging applications (AI, IoT, etc.)
Production Efficiency	Focused on cost efficiency for mass production	Focused on agility, shorter lead times, and adaptability

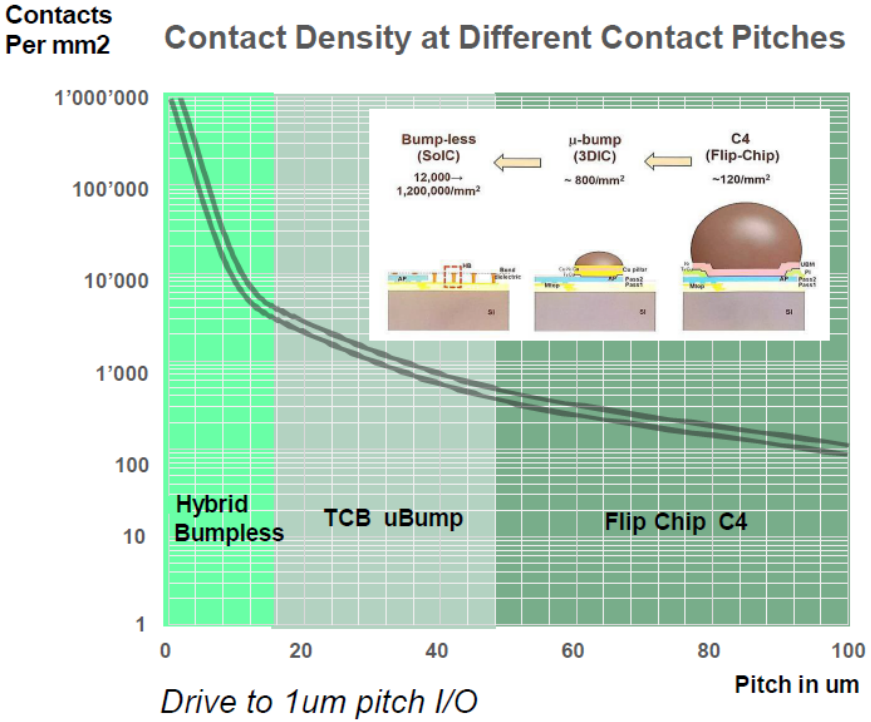
Features of Foundry 2.0



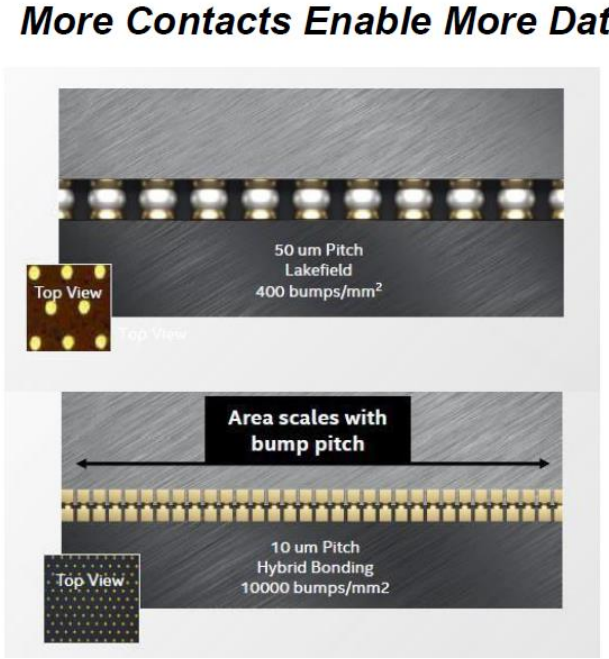
Contributions & Benefits of Foundry 2.0

Role	Key Contributions	Benefits
Wafer-Level Packaging (WLP)	- Provides high-density interconnections for compact designs. - Enables modular and scalable integration.	- Higher interconnect density. - Reduced production costs with wafer-level assembly. - Enhanced thermal performance.
Chiplet-Based Architectures	- Enables modular designs with scalability for HMLV markets. - Facilitates heterogeneous integration for multi-functionality.	- Reduced design complexity for advanced systems. - Lower production costs for custom chips. - Enhanced system performance.
Defect Detection and Quality Assurance	- Implements advanced non-destructive testing to identify nanometer-scale defects. - Uses AI for predictive analytics and anomaly detection.	- Reduced defect rates and improved yield. - Faster detection of structural defects and voids. - Higher product reliability.
Collaboration and Customization	- Develops customized packaging solutions for niche applications like AI, IoT, and automotive. - Aligns with IDM product roadmaps for future tech integration.	- Faster time-to-market. - Greater alignment with emerging technologies. - Better ecosystem integration.
Sustainability and Efficiency	- Reduces material waste and energy consumption. - Simulates manufacturing workflows to enhance efficiency.	- Lower environmental impact. - Cost-efficient operations. - Compliance with sustainability regulations.

Hybrid Bonding Innovation

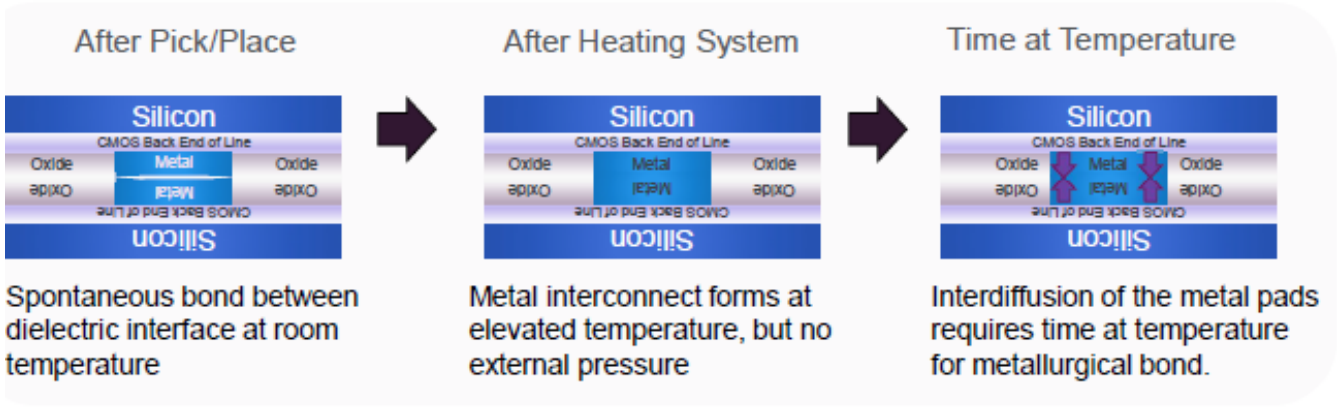


Tom Strothman, BESI

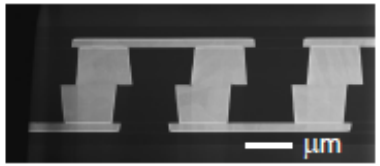


Intel

Mechanism for Hybrid Bonding



Cross Section

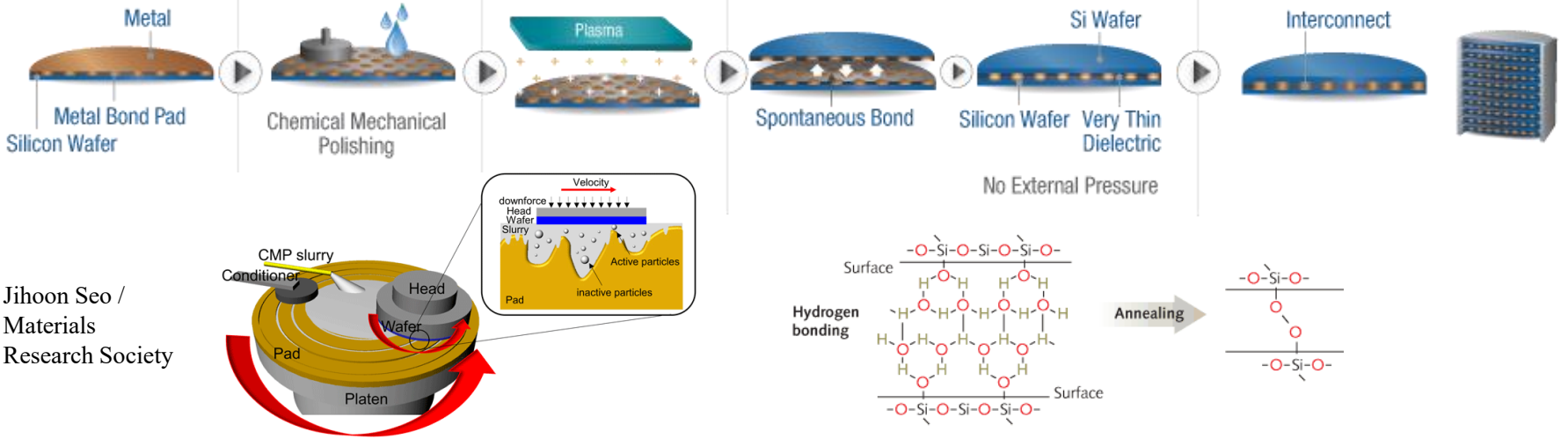


Features

Bond Metal	Cu, Ni
Bond Pad Size	<1um to 20um
Low Temperature	~150 – 400°C
Compatible Dielectrics	Si_xO_y, $Si_xO_yN_z$, $Si_xC_yN_z$

adeia Gillian Gao

DBI®: Low Temperature Hybrid Bonding Process



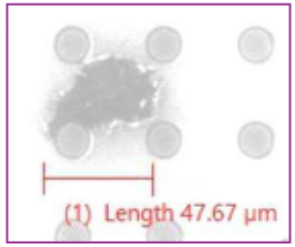
Jihoon Seo / Materials Research Society

Intrinsic Yield Loss Mechanisms for Hybrid Bonded Chiplets

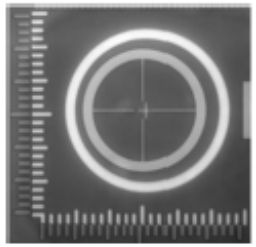
Potential Sources of Yield Loss

#	Defect	Cause
1	Void	Environmental Particles / Manual Handling
2	Void	Dicing / Edge Quality
3	Void	Bonder Related: Eject, Flip, Gantry motion
4	Misalignment	Die Shift / Die Rotation / Deformation
5	Cracked Die	Thin Die (≤ 50 mm) Unoptimized Singulation or Ejection
6	Unconnected bond pads	Excessive Recess / Recess Variation Insufficient Anneal
7	Intrinsic Defects	Defects in metal stack Not related to hybrid bond

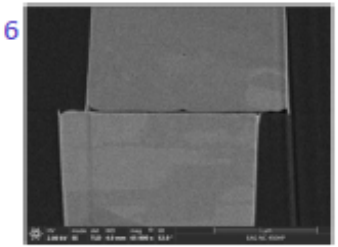
Root Cause Failure Mode Examples



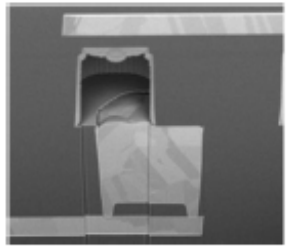
Particle causing Void



Misalignment



Excessive Recess



Intrinsic Defect

Reference: T. Workman et al., ECTC May 2023

Metrologies for Hybrid Bonding

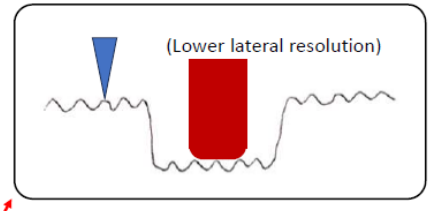
AFM for bonding surface characterization – Topography measurements

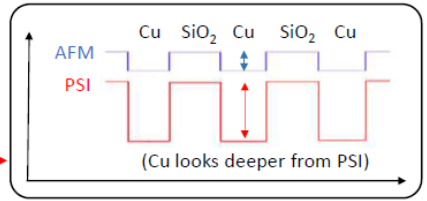
Phase Shift Interferometry (PSI) – Optical interferometry that is 1000X faster than AFM

Wafer-Level recess distribution

CSAM for Bonding Interface Void Detection

Characteristics Comparison	AFM 	PSI 
Acquisition time per image	Minutes	Seconds
Imaging size	< 100 µm	300 µm - 4 mm
Time to image an example 200mm wafer	> 5 years	~ 1 day
Topography resolution (z)	< 0.1 nm	~ 1 nm
Lateral resolution (xy)	~ 5 nm	~ 500 nm
Sample dependency	No	Depends on refractive index, etc. → Needs calibration

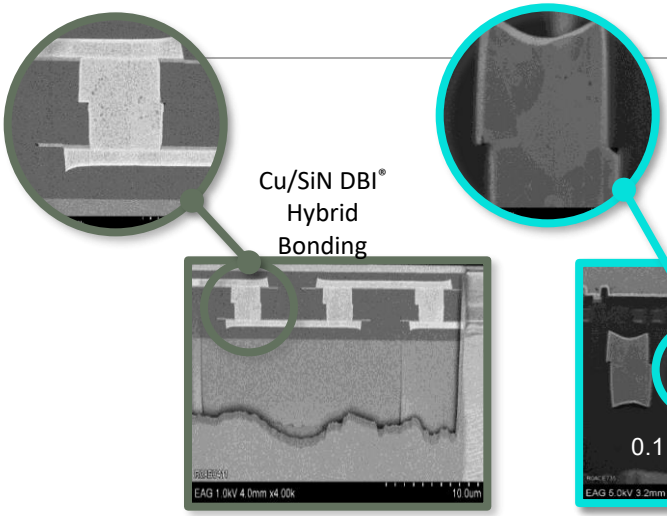




- Atomic force microscopy (AFM): Standard technique for hybrid bond topography measurements
- Optical interferometry: Phase-Shift Interferometry (PSI) is > 1000x faster, but has limitations

Reference: B Lee, “Hybrid Bonding in Advanced Heterogeneous Integration: Key Metrology Enablers”, ICSJ 2024, Kyoto, Japan

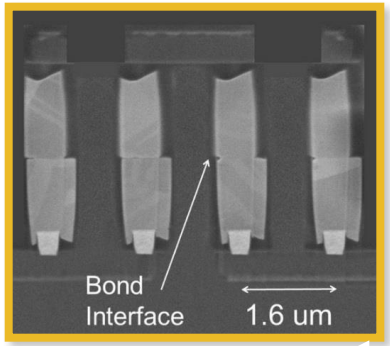
Hybrid Bonding Interconnect Pitch Scaling



10 µm DBI® pitch, 300℃

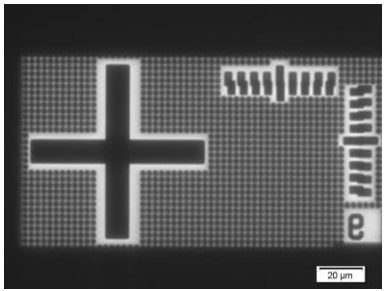
1.9 µm DBI® pitch, 300℃

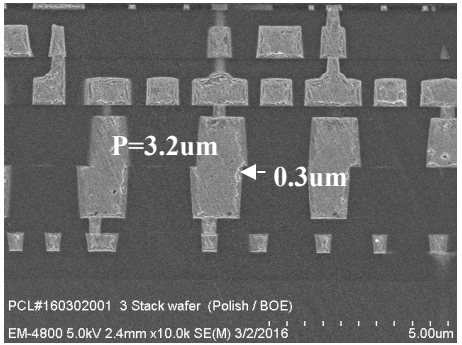
Scalable To < 1um Pitch
0.8um Pitch Demonstrated



1.6 µm DBI® pitch, 300℃

- WtoW 3sigma < ±1um misalign performance
- DtoW 3sigma < ±200nm misalign performance
- Production Minimum pitch = 2.44um
- Best alignment is achieved with face-to-face bonding





Quality Assurance in Advanced Packaging

- Quality assurance (QA) is a vital component of advanced packaging, ensuring the reliability and performance of semi- conductor devices.
- Integrating **AI-driven defect detection** techniques can improve the accuracy and efficiency of U.S. manufacturing processes.
- This approach will not only elevate the quality of U.S. semiconductor products but also strengthen their position in the global market, reinforcing the importance of cross-border learning and innovation.

Defect Detection Innovation

- One of out-source assembly & test (OSAT) primary contributions to defect detection innovation is their ability to integrate state-of-the-art inspection tools such as automated optical inspection (AOI), automated X-ray inspection (AXI), and SEM into high-volume manufacturing environments.
- Moreover, OSATs are driving the adoption of AI and machine learning (ML) in defect detection.
- OSATs foster innovation by providing a collaborative platform for ecosystem partners, including foundries, equipment manufacturers, and research institutions.
- Finally, OSAT facilities play a strategic role in standardizing defect detection practices across the semiconductor industry.

Strategic Path Forward for the U.S.

- The transition to Foundry 2.0 and the growth of OSAT facilities necessitate substantial infrastructure investments and strategic planning to keep pace with advancements in semiconductor technology.
- While the U.S. government semiconductor policies are pivotal in bolstering domestic capabilities, similar initiatives are gaining momentum globally.
- These global efforts highlight the importance of international collaboration and regional specialization in advanced packaging and WLP. For example, the European Chips Act provides funding for research into next-generation packaging technologies and promotes cross-border partnerships among member states.

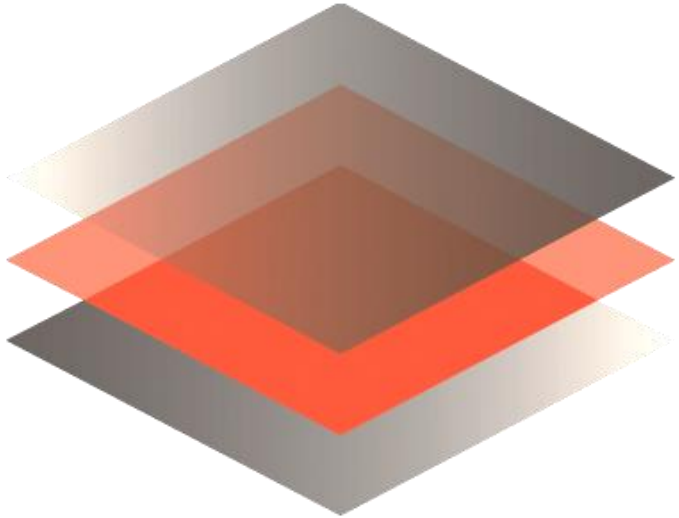
Global Insights to Local Action

- Taiwan's success in heterogeneous integration and South Korea's leadership in high-bandwidth memory (HBM) technologies illustrate the impact of concentrated R&D efforts.
- For U.S. OSATs, adapting these global best practices requires establishing collaborative research hubs that focus on addressing unique technical challenges such as interconnect density, thermal management, and yield optimization in WLP.
- By focusing on R&D that emphasizes agility and niche market applications—such as automotive and aerospace semiconductors U.S. OSATs can redefine their role in the global semiconductor supply chain.

Summary

- The U.S. OSAT sector is at a critical inflection point, with the opportunity to establish itself as a key contributor to the global semiconductor industry.
- U.S. OSATs must prioritize investments in state-of-the-art packaging technologies, including 2.5D/3D integration, WLP, and chiplet architectures.
- Equally critical is the integration of AI-driven test solutions and big data analytics into testing frameworks.
- Collaboration is a fundamental pillar of this strategy. Strengthening partnerships with IDMs, fabless companies, and academic institutions will ensure that packaging and testing innovations align with upstream design requirements and downstream market demands.

THANK YOU!



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