A Global View Versus a U.S. Focus on Outsourced Assembly and Test (OSAT) Facilities to Support Wafer Level Packaging

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***Abstract*—The semiconductor industry is experiencing a paradigm shift from the traditional Foundry 1.0 model, centered on low-mix, high-volume production, to the collaborative and agile Foundry 2.0 paradigm. This transformation places Outsourced Assembly and Test (OSAT) facilities at the forefront of modern semiconductor manufacturing, with wafer-level packaging (WLP) emerging as a critical technology to address the power, performance, and density demands of applications such as artificial intelligence (AI), 5G, and autonomous systems.**

This paper examines the strategic roles of global leaders in Asia, who have leveraged advanced 2.5D / 3D integration, chiplet architectures, and AI-driven defect detection to establish dominance. Comparatively, the U.S. faces unique challenges, including fragmented supply chains and limited domestic infrastructure. However, the CHIPS and Science Act offers a pivotal opportunity to revitalize U.S. OSATs by supporting investments in state-of-the-art technologies, workforce development, and sustainability practices.

The discussion extends to integrating AI and big data analytics in defect detection, enhancing scalability and yield optimization, and the importance of adopting global best practices tailored to the U.S. context. Furthermore, ecosystem collaboration with Integrated Device Manufacturers (IDMs), fabless companies, and academia is emphasized as a cornerstone for aligning innovations with industry requirements. Quality assurance frameworks, sustainability goals, and regional specialization are also explored as critical enablers of resilience and competitiveness.

Through a comprehensive roadmap, this paper provides actionable insights for US OSATs to close the gap with global leaders, establish technological leadership, and ensure a robust and secure semiconductor ecosystem capable of addressing the challenges of a rapidly evolving landscape.

***Index Terms*—Foundry 1.0, Foundry 2.0, Wafer Level Packaging, OSATs, Chiplets and Advanced Packaging.**

I. Introduction

The semiconductor industry is undergoing a profound transformation, transitioning from the rigid Foundry 1.0 model to the dynamic, collaborative framework of Foundry 2.0 [1]. At the heart of this evolution is the OSAT facility, which has emerged as a critical enabler of advanced WLP technologies [2]. These technologies address the increasing demands for power efficiency, performance, and density in next-generation applications such as artificial intelligence (AI), 5G, and autonomous systems.

Globally, semiconductor giants in Asia have established dominance in OSAT-driven innovations, leveraging expertise in 2.5D/3D integration, chiplet architectures, and AI-driven defect detection [3]. These advancements have allowed these nations to maintain leadership in heterogeneous integration and modular semiconductor designs. In contrast, the United States faces unique challenges, including fragmented supply chains, limited domestic infrastructure, and the lack of coordinated strategies for integrating advanced WLP into its semiconductor ecosystem [4]. Figure 1 highlights the suppliers of critical materials used in WLP, with only a handful of companies operating from the U.S.

The enactment of the CHIPS and Science Act marks a pivotal moment for the U.S. semiconductor industry, providing a framework to address these gaps [5]. Strategic investments in state-of-the-art technologies, workforce development, and sustainable manufacturing practices offer an opportunity to realign U.S. OSAT facilities with global best practices. However, achieving competitiveness requires more than policy support; it demands a comprehensive strategy to leverage global innovations while tailoring them to the U.S. technology needs.

This paper explores the strategic contrast between the global dominance of OSAT facilities, especially regions in Asia, and the evolving U.S. focus on rebuilding its semiconductor manufacturing ecosystem with a focus on advanced packaging. It examines how advanced WLP technologies can serve as a foundation for competitiveness, addressing domestic and global market demands. The analysis delves into the integration of AI-driven defect detection and big data analytics to enhance scalability, yield optimization, and operational efficiency in OSAT processes.

By providing actionable insights, this study outlines a roadmap for U.S. OSAT facilities to close the gap with global leaders. The roadmap emphasizes ecosystem collaboration with Integrated Device Manufacturers (IDMs), fabless companies, and academia to align U.S. innovations with industry requirements. Furthermore, it discusses the need for adopting global best practices, such as modular packaging designs and sustainability-focused manufacturing, while addressing localized challenges like labor costs and supply chain resilience.

Through this comparative analysis and forward-looking recommendations, this paper aims to bridge the gap between the global view and the U.S. focus on OSAT capabilities, offering a pathway for the U.S. to achieve leadership in wafer-level and advanced packaging semiconductor manufacturing. This holistic approach ensures the development of a robust, secure, and globally competitive semiconductor ecosystem.

II. The current landscape of Semiconductor Manufacturing: Foundry 1.0

A. Characteristics of Foundry 1.0

The Foundry 1.0 model epitomizes the traditional low- mix, high-volume (LMHV) approach to semiconductor manufacturing, prioritizing transistor scaling for mass production [6]. This model, dominant for decades, drove unprecedented advancements in performance, power efficiency, and integration density by continually reducing transistor dimensions. These gains catalyzed breakthroughs in computing, telecommunications, and consumer electronics, transforming global industries. However, its reliance on standardized, high-output production struggled to address the diverse demands of emerging high-mix, low-volume (HMLV) applications such as AI, the IoT, and edge computing [7].

Globally, LMHV practices thrived in countries with ro- bust resources and established semiconductor ecosystems, particularly countries in Asia, where massive investments bolstered competitive scaling [8]. Conversely, the U.S. encountered challenges in sustaining relevance due to the capital intensity of LMHV manufacturing and its inability to nimbly address HMLV market segments. The high costs of designing, fabricating, and scaling smaller nodes often excluded smaller or niche-market companies, further consolidating the power among global leaders.

This rigidity was exacerbated by the "kitchen sink" approach, which included monolithic chip designs packed with excessive functionalities to suit broader markets. While versatile, these designs often led to inefficiencies in power consumption, cost, and space utilization, leaving them ill-suited for specialized HMLV applications like AI and IoT [9]. Such markets demanded tailored, flexible solutions that the Foundry 1.0 paradigm, with its LMHV focus, could not provide.

Despite its limitations, Foundry 1.0 established the foundation for modern semiconductor manufacturing, enabling transformative innovations like advanced packaging and heterogeneous integration. However, the inherent limitations of LMHV production underscored the critical need to shift to a more agile, collaborative HMLV-capable model. This transition, embodied by Foundry 2.0 requires OSAT facilities to address the challenges of flexibility, customization, and efficiency left unresolved by Foundry 1.0.

B. Limitations of the Foundry 1.0 Approach

While the Foundry 1.0 model revolutionized semiconductor manufacturing through LMHV production, its focus on generalized chip designs revealed significant shortcomings as technological demands diversified. Emerging markets, driven by HMLV applications such as AI, the IoT, and edge computing, required far greater flexibility and customization than LMHV could offer. This limitation left niche markets underserved, creating a widening gap between industry needs and the Foundry 1.0 approach.

One of the critical drawbacks of the model was its capital-intensive nature. The construction of state-of-the-art facilities required billions in investment and substantial nonrecurring engineering (NRE) costs, effectively sidelining smaller companies [10]. This concentrated manufacturing dominance among key players in Asia, while the U.S. struggled with limited government support and fragmented supply chains, further eroded its competitive position.

Additionally, the rigid processes of LMHV production hindered efficiency in addressing specialized, application-specific needs. Foundry 1.0 excelled at scaling for general-purpose chips but lacked the agility required to adapt quickly to emerging demands. This inflexibility became a bottleneck, especially as industries moved toward tailored designs for cutting-edge technologies.

Moreover, Foundry 1.0's siloed workflows hindered collaboration among designers, manufacturers, and suppliers, slowing the pace of innovation in areas like advanced packaging and defect detection. These inefficiencies underscored the growing need for a paradigm shift—one that prioritizes agility, integration, and HMLV strategies.

The evolution to Foundry 2.0 marks a decisive step forward. By embracing ecosystem-driven innovation and leveraging the expertise of OSAT facilities, Foundry 2.0 addresses the customization, flexibility, and efficiency challenges that Foundry 1.0 could not overcome. This transition sets the stage for a semiconductor industry equipped to meet the demands of emerging technologies with precision and adaptability.

III. The Emerging Paradigm: Foundry 2.0

A. Introduction to Foundry 2.0 – The Future Direction of NHanced Semiconductors

The limitations of Foundry 1.0 have paved the way for the emergence of a transformative manufacturing paradigm: Foundry 2.0. Table I. clearly outlines the different operating models of Foundry 1.0 and Foundry 2.0. In the case of Foundry 2.0, unlike its predecessor, which centered on LMHV production, Foundry 2.0 embraces the agility and customization of HMLV strategies. This shift is driven by the growing demand for specialized solutions in areas like AI, the IoT, and 5G, where flexibility and integration are paramount [11].

At its core, Foundry 2.0 fosters collaboration, breaking down silos to create an interconnected ecosystem that brings designers, manufacturers, and OSAT facilities into closer alignment as represented in Figure 2. OSATs take on a pivotal role by offering advanced WLP, precise defect detection, and modular assembly services, empowering manufacturers to focus on innovation. This collaborative framework makes Foundry 2.0 uniquely capable of addressing rapidly evolving technological needs, particularly in markets that prioritize performance, efficiency, and compact design.

We believe that global semiconductor leaders will have to embraced this model to maintain their competitive edge.

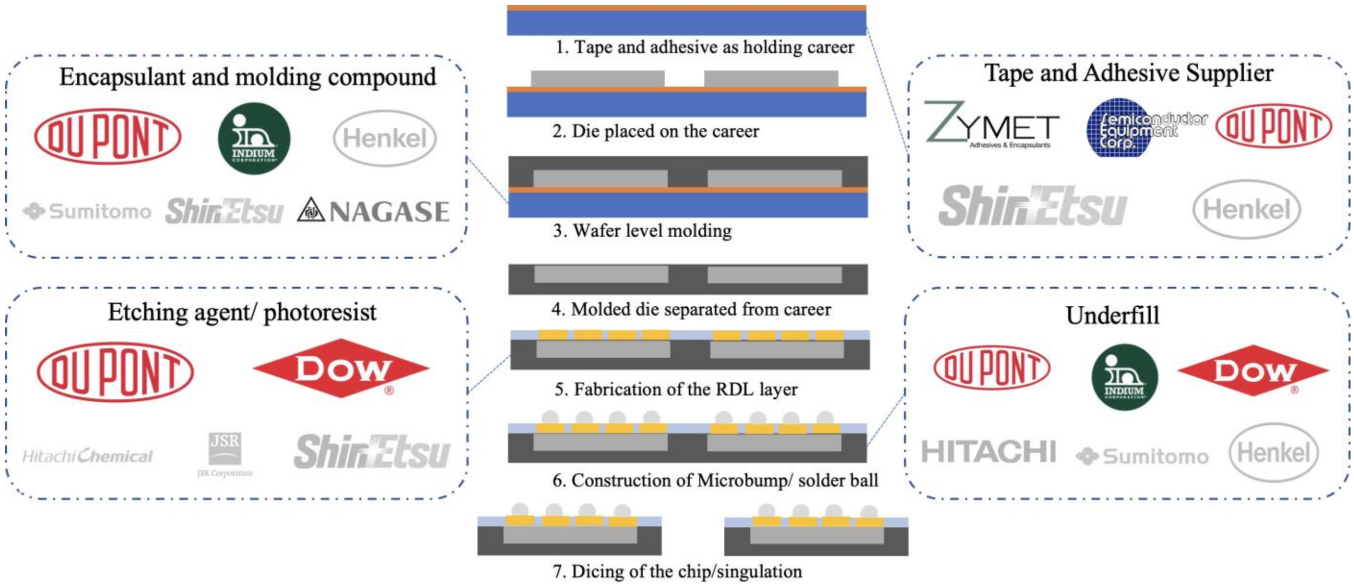

Fig. 1. Onshore and Offshore (grey-colored) suppliers of WLP in the U.S.
[12]

In contrast, the U.S. has historically faced challenges due to fragmented supply chains and insufficient investment. However, government initiatives are now accelerating the country's shift toward Foundry 2.0 principles [13]. By aligning domestic OSAT facilities with global best practices and fostering innovation, the U.S. has an opportunity to strengthen its semiconductor ecosystem while building resilience in its supply chains.

The NHanced Foundry 2.0 approach represents more than a mere evolution of manufacturing practices—it is a necessary response to the complex demands of modern technologies. By leveraging the HMLV approach and fostering ecosystem-driven innovation, it offers the flexibility, customization, and efficiency needed to propel the semiconductor industry into a more specialized and interconnected future.

B. Strategic Advantages of the Foundry 2.0 Model

Building on the foundational shifts introduced by Foundry 2.0, this model offers transformative advantages that address the limitations of its LMHV predecessor. By emphasizing HMLV production [14], Foundry 2.0 enables manufacturers to develop application-specific solutions optimized for emerging technologies such as AI, the IoT, and 5G. This tailored approach ensures that the industry can adapt to the growing demand for performance, power efficiency, and cost-effective designs, which were previously unattainable with the monolithic strategies of Foundry 1.0.

Central to Foundry 2.0's success is its ecosystem-driven collaboration model. Unlike the siloed workflows of Foundry 1.0, this paradigm fosters real-time integration among designers, manufacturers, and OSAT facilities, creating a streamlined process that accelerates innovation. OSATs are pivotal in this ecosystem, driving advanced packaging techniques like chiplet-based architectures and 2.5D/3D integration. These modular and scalable solutions extend the benefits of Moore's Law while minimizing production costs and enhancing product performance.

Sustainability also emerges as a key advantage of Foundry 2.0, reflecting the industry's growing focus on environmental stewardship. By leveraging AI-driven defect detection and digital twin technologies, OSATs help optimize resource utilization and reduce material waste, meeting regulatory expectations while appealing to environmentally conscious consumers. This alignment with sustainability goals not only enhances competitiveness but also positions Foundry 2.0 as a forward-looking model capable of meeting global challenges.

For the U.S., Foundry 2.0 represents a strategic opportunity to regain semiconductor leadership. While Asian countries have long championed the LMHV model, recent investments under the CHIPS and Science Act are enabling the U.S. to align domestic OSAT facilities with global best practices to create an optimized chiplet manufacturing infrastructure onshore [15]. By prioritizing infrastructure development, workforce training, and collaborative innovation, the U.S. is enhancing supply chain resilience and ensuring technological independence in an increasingly competitive landscape.

In essence, Foundry 2.0 transcends the boundaries of traditional manufacturing by delivering flexibility, fostering collaboration, and aligning with sustainability goals. This paradigm equips the semiconductor industry to meet the demands of modern technology while addressing the shortcomings of the past, ensuring a resilient and competitive future.

C. Key players and Potential Partners

The Foundry 2.0 model is transforming semiconductor manufacturing, with WLP emerging as a cornerstone of this

TABLE I
COMPARISON OF FOUNDRY 1.0 AND FOUNDRY 2.0 IN SEMICONDUCTOR MANUFACTURING

Aspect	Foundry 1.0	Foundry 2.0
Production Model	Low-Mix High Volume	High-Mix Low Volume
Key Features	Pure-play fabrication services	Design support, heterogeneous integration, and innovation
Packaging	Monolithic chips	Chiplet-based architectures, 2.5D/3D integration
Market Strategy	Low Mix, High Volume: Mass production of standardized chips for broad applications.	High Mix, Low Volume: Production of customized, application-specific chips for niche and emerging markets.
Collaboration Model	Isolated operations, minimal designer-foundry interaction	Ecosystem-driven real-time collaboration across stakeholders
Government Support	Limited support; industry-driven	Backed by government initiatives across the world and CHIPS Act in the U.S.
Flexibility	Low, focused on broad markets	High, with adaptability for emerging applications (AI, IoT, etc.)
Production Efficiency	Focused on cost efficiency for mass production	Focused on agility, shorter lead times, and adaptability

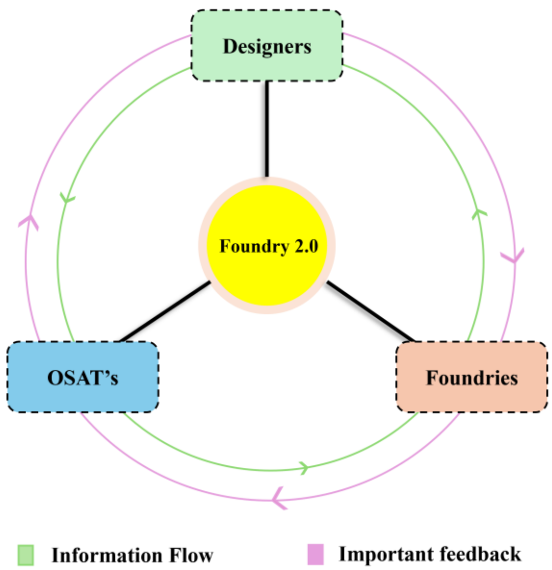

Fig. 2. Critical features of Foundry 2.0 in driving increased collaboration and flexibility

evolution. This paradigm relies heavily on OSAT facilities to support HMLV production and advanced packaging technologies, addressing the demands of application-specific markets such as AI, the IoT, and 5G. Globally, nations in Asia have established themselves as leaders in WLP innovation, leveraging strong OSAT ecosystems to deliver cutting-edge solutions [16]. For instance, TSMC (Taiwan Semiconductor Manufacturing Company) integrates WLP techniques like fan-out wafer-level packaging (FOWLP) as shown in Figure 3, and chiplet-based architectures to enhance performance, power efficiency, and scalability [17]. Similarly, Samsung Electronics combines its memory and logic expertise with 2.5D and 3D integration, excelling in both mass-market and niche applications [18]. In East Asia, Semiconductor Manufacturing International Corporation (SMIC) and OSAT leader JCET are advancing fan-in and fan-out packaging for sectors such as automotive and IoT, while ASEAN (Association of Southeast Asian Nations) countries are emerging as key hubs for cost-effective and high-reliability OSAT services.

In contrast, the U.S. semiconductor industry has historically lagged in its adoption of WLP and advanced packaging capabilities due to fragmented supply chains and limited infrastructure. While global leaders excel in integrating WLP into their packaging strategies, U.S. efforts have been constrained by gaps in expertise and coordination. However, the recently unveiled government initiatives provided a pathway for revitalization. Companies like Intel and GlobalFoundries are leading the charge, with Intel's IDM 2.0 strategy prioritizing partnerships with OSAT providers to adopt advanced WLP solutions [19], and GlobalFoundries focusing on tailored packaging for critical industries like automotive and healthcare. These efforts are bolstered by government investment and a growing emphasis on workforce training, positioning the U.S. to strengthen its OSAT ecosystem and compete globally.

A notable example of the U.S. semiconductor industry's revitalization is the strategic collaboration between TSMC and Amkor Technology in Arizona. TSMC's establishment of a state-of-the-art semiconductor fabrication facility, coupled with Amkor's expertise in OSAT services, represents a synergistic partnership driving innovation in advanced packaging technologies. This collaboration strengthens the integration of WLP into the Foundry 2.0 framework, serving as a cornerstone for localizing critical components of the semiconductor supply chain. Bolstered by U.S. government support, this partnership addresses longstanding challenges in fragmented supply chains and aligns U.S.-based production with global standards for technological resilience, efficiency, and competitiveness. By leveraging both entities' complementary strengths, this collaboration fosters an ecosystem capable of meeting the demands of emerging technologies such as AI, 5G, and the IoT.

Beyond established players, niche innovators worldwide are shaping the WLP landscape. European companies such as ASML and Soitec provide photolithography and advanced wafer solutions that enable WLP at scale, while startups like California's Flex Logix Technologies are advancing energy-efficient chipset architectures [20]. Sustainability also plays a crucial role in Foundry 2.0's adoption, with companies like Applied Materials and Lam Research leading efforts to reduce energy consumption and material waste through AI-driven defect detection and digital twin technologies.

The global contributions to Foundry 2.0 underscore the importance of collaboration in advancing WLP capabilities. While Asian countries continue to lead in innovation, the U.S. is taking significant steps to close the gap, leveraging government support and cross-border partnerships. This interconnected approach ensures that the semiconductor industry can meet the demands of emerging technologies while fostering resilience, customization, and sustainability.

IV. Collaboration with IDMs and Fabless Companies

Collaboration with IDMs and fabless companies is pivotal for U.S. OSAT facilities to advance WLP technologies and address the growing demand for high-performance applications in AI, 5G, and autonomous systems [21]. These partnerships ensure that innovations in 2.5D/3D integration, chiplet architectures, and advanced packaging are developed in alignment with evolving industry requirements, enabling U.S. OSATs to compete globally.

Joint research and development (R&D) initiatives represent a crucial mechanism for fostering such collaborations. Global leaders like TSMC and AMD have demonstrated the success of co-developing chiplet-based CPUs [22], resulting in significant performance and efficiency gains. U.S. OSATs can replicate this model by partnering with domestic fabless companies like Qualcomm and NVIDIA to create tailored WLP solutions that meet the unique demands of next-generation applications. By prioritizing such partnerships, U.S. OSATs can accelerate innovation cycles and strengthen their relevance in the semiconductor value chain.

Co-development agreements further enable alignment between U.S. OSAT capabilities and IDM product roadmaps. For example, Intel's IDM 2.0 strategy highlights the importance of integrating advanced WLP processes into processor designs. These agreements ensure that U.S. OSATs are equipped to support the specific performance, power, and density requirements of future technologies, reducing the dependency on foreign OSAT ecosystems.

Additionally, active participation in consortia such as the Semiconductor Research Corporation (SRC) and the International Semiconductor Manufacturing Initiative (ISMI) provides U.S. OSATs with access to cutting-edge expertise and best practices [23]. Collaborative platforms like these are essential for pooling resources and advancing AI-driven defect detection and sustainable WLP practices. By adopting global best practices while addressing local priorities, U.S. OSATs can build robust packaging capabilities that enhance both efficiency and competitiveness.

These strategic collaborations are key to reducing the reliance on foreign supply chains and fostering resilience within the U.S. semiconductor ecosystem. Supported by government policies, the U.S. OSATs have the opportunity to establish a leadership role in WLP, ensuring they are well-positioned to meet domestic and global demand for advanced semiconductor packaging.

V. Opportunities in Advanced Packaging and Chiplet Architecture

A. *The Role of Advanced Packaging*

Advanced packaging has become a cornerstone of semiconductor innovation, driven by a global ecosystem where regional strengths complement one another. Global leaders like TSMC (Taiwan), Samsung (South Korea), and Amkor Technology (U.S.) have pioneered advanced packaging solutions, setting benchmarks in cost efficiency and performance. While TSMC dominates in 2.5D and 3D integration, and Samsung in high-bandwidth memory (HBM) packaging, U.S.-based OSATs have a unique opportunity to adapt and leverage these innovations to strengthen domestic capabilities.

U.S. OSATs, supported by government initiatives, can integrate lessons from global leaders to advance WLP and chiplet architectures. For instance, TSMC's expertise in heterogeneous integration and modular designs can guide U.S. firms in optimizing processes for diverse applications, from AI to IoT. By adopting these globally tested strategies, U.S. facilities can not only enhance their competitiveness but also reduce reliance on foreign supply chains, ensuring resilience in times of geopolitical uncertainty.

B. *Chiplet-Based Architectures for U.S OSAT's*

Chiplet-based architectures have emerged as a transformative solution to the growing complexities of modern semiconductor manufacturing, addressing both technical and economic challenges. By enabling modularity and scalability, chiplets support HMLV applications while reducing design and production costs. Advanced technologies like 2.5D integration, 3D stacking, and WLP play a pivotal role in this shift, reshaping global and U.S. OSAT capabilities to meet the demands of AI, 5G, and IoT [24].

Globally, Asian semiconductor companies have set benchmarks in leveraging 2.5D and 3D integration. Taiwan's TSMC, for example, has championed silicon interposer technologies to interconnect chiplets with high bandwidth and low latency, while South Korea's Samsung has excelled in 3D stacking [25], enabling dense integration of logic and memory dies for compact, high-performance designs. These advances underscore the role of OSATs in providing high-reliability solutions for diverse markets.

In contrast, U.S. OSATs are at a critical juncture. Historically hindered by fragmented supply chains and limited infrastructure [26], they now have the opportunity to adopt and adapt these global innovations. With the support of initiatives, the U.S. OSATs can invest in hybrid bonding, advanced through-silicon vias (TSVs), and fan-out WLP to bolster their competitive edge. The adoption of these technologies not only enhances scalability and performance but also positions U.S. OSATs as key players in critical industries like aerospace, defense, and healthcare.

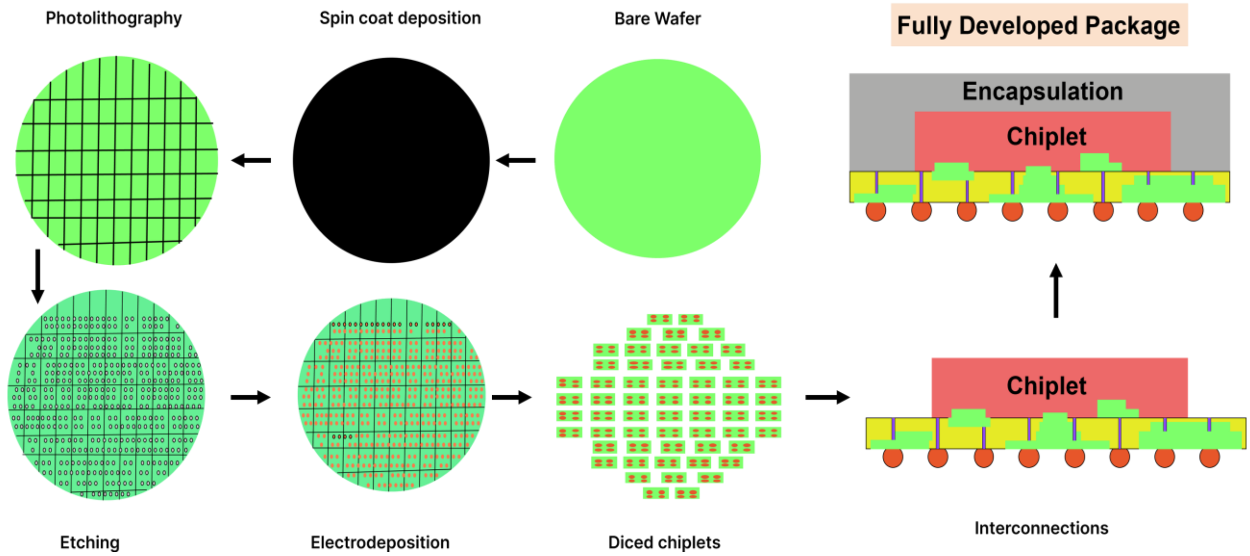

Fig. 3. FOWLP Process for Creation of Advanced Packages

Moreover, the modularity of chiplet architectures aligns with the flexibility required by emerging markets. Wafer- level packaging, in particular, offers scalability by enabling much of the assembly process at the wafer level, minimizing production overheads while maximizing throughput [27]. Fan-out WLP provides the additional advantage of higher interconnect density, essential for chiplets used in advanced computing applications [28]. By integrating these technologies with AI-driven defect detection, U.S. OSATs can achieve greater precision and yield optimization, meeting the rigorous demands of cutting-edge semiconductor applications [29].

The benefits of chiplet-based architectures extend beyond technical performance. For U.S. OSATs, they represent an opportunity to redefine their role within the global semiconductor ecosystem by blending global best practices with localized priorities by adopting a Foundry 2.0 model. Through investments in advanced technologies, workforce training [30], and strategic collaboration, the U.S. semiconductor industry can transition from a position of catching up to one of leadership. By embracing these advancements, U.S. OSATs will not only enhance their ability to support wafer-level packaging but also ensure resilience and innovation in a rapidly evolving landscape.

C. Role of OSATs in Foundry 2.0 and WLP

In the Foundry 2.0 ecosystem, U.S. OSATs have a critical role in bridging global innovations with domestic manufacturing priorities. By incorporating practices from leaders like ASE Group (Taiwan) and JCET (China), U.S. facilities can advance in areas such as fan-in and fan-out WLP, wafer stacking, and high-density interconnects. These technologies, when adapted for U.S. needs, can support sectors like aerospace, automotive, and defense, which demand high-reliability semiconductor solutions [31]. Table II provides an overview of OSAT's contributions to advanced packaging, highlighting key roles such as wafer-level packaging, chiplet-based architectures, and sustainability initiatives.

Additionally, U.S. OSATs can foster collaborative partnerships with international leaders to develop hybrid models that blend global expertise with local priorities. For instance, joint ventures focused on 3D packaging for AI processors could position U.S. OSATs as integral players in the next wave of semiconductor innovation [32]. Such efforts would also strengthen the resilience of the domestic supply chain, reducing vulnerabilities to global disruptions.

D. Quality Assurance in Advanced Packaging

Quality assurance (QA) is a vital component of advanced packaging, ensuring the reliability and performance of semiconductor devices [33]. By learning from global QA practices, U.S. OSATs can enhance their inspection methods. For example, integrating AI-driven defect detection techniques used by JCET and ASE Group can improve the accuracy and efficiency of U.S. manufacturing processes. Similarly, adopting advanced scanning acoustic microscopy (SAM) techniques can help U.S. facilities address challenges in bonded interfaces and multilayered structures.

Through these adaptations, U.S. OSATs can build on global best practices to develop a robust QA framework that meets domestic and international standards. This approach will not only elevate the quality of U.S. semiconductor products but also strengthen their position in the global market, reinforcing the importance of cross-border learning and innovation.

VI. AI-Driven Test Solutions and Big Data Analytics

A. Enabling Advanced OSAT Capabilities

The integration of AI-driven test solutions and big data analytics represents a transformative shift for OSAT facilities, enabling them to meet the demands of increasingly complex

TABLE II
OVERVIEW OF OSAT'S CONTRIBUTION TO ADVANCED PACKAGING

Role	Key Contributions	Benefits
Wafer-Level Packaging (WLP)	- Provides high-density interconnections for compact designs. - Enables modular and scalable integration.	- Higher interconnect density. - Reduced production costs with wafer-level assembly. - Enhanced thermal performance.
Chiplet-Based Architectures	- Enables modular designs with scalability for HMLV markets. - Facilitates heterogeneous integration for multi-functionality.	- Reduced design complexity for advanced systems. - Lower production costs for custom chips. - Enhanced system performance.
Defect Detection and Quality Assurance	- Implements advanced non-destructive testing to identify nanometer-scale defects. - Uses AI for predictive analytics and anomaly detection.	- Reduced defect rates and improved yield. - Faster detection of structural defects and voids. - Higher product reliability.
Collaboration and Customization	- Develops customized packaging solutions for niche applications like AI, IoT, and automotive. - Aligns with IDM product roadmaps for future tech integration.	- Faster time-to-market. - Greater alignment with emerging technologies. - Better ecosystem integration.
Sustainability and Efficiency	- Reduces material waste and energy consumption. - Simulates manufacturing workflows to enhance efficiency.	- Lower environmental impact. - Cost-efficient operations. - Compliance with sustainability regulations.

semiconductor designs. As WLP technologies advance, the role of precise, efficient, and scalable testing methodologies becomes pivotal in ensuring reliability and competitiveness. While traditional testing frameworks often struggle to keep pace with the miniaturization and complexity of modern integrated circuits (ICs), AI and big data analytics provide OSATs with the tools to revolutionize defect detection, yield optimization, and overall efficiency [34].

B. Technical Implications of AI-Driven Test Solutions

AI-driven test solutions leverage machine learning models and advanced algorithms to identify defects at nanometer- scale resolutions, far beyond the capabilities of conventional testing methods [35]. For example, deep learning models can process data from X-ray imaging, scanning electron microscopy (SEM), and other non-destructive testing techniques to detect anomalies in multi-layered semiconductor packages [36]. These solutions are particularly effective in addressing challenges such as identifying voids, delamination, and micro-cracks within 2.5D and 3D integration structures [37].

Moreover, AI enables real-time defect classification and predictive analytics, allowing OSATs to proactively address manufacturing variations before they impact yield. Reinforcement learning techniques can be applied to optimize test patterns and coverage, reducing the time and cost associated with exhaustive testing protocols. For instance, by training AI models on historical defect patterns, OSATs can prioritize high-risk areas of IC packages, ensuring that testing resources are allocated efficiently [38].

C. Practical Applications of Big Data Analytics

Big data analytics amplifies the value of AI-driven testing by processing the massive volumes of data generated during semiconductor manufacturing. OSATs can use these insights to refine process parameters, monitor equipment performance, and identify long-term trends in defect occurrence [39]. This data-driven approach not only enhances product quality but also enables continuous process improvement, aligning with the agility and customization demands of Foundry 2.0 [40].

For example, advanced analytics tools can aggregate data from diverse sources, including inspection equipment, manufacturing environments, and test results, to identify correlations between process variables and defect rates. These insights allow engineers to implement targeted adjustments, reducing variability and improving yield. Additionally, big data analytics supports the development of digital twins—virtual models of physical processes—which enable OSATs to simulate and optimize manufacturing workflows without disrupting live operations [41].

D. U.S. OSAT Competitiveness Through AI and Big Data

For U.S. OSATs, the adoption of AI and big data analytics provides a competitive advantage against global leaders. While Asian countries have successfully integrated these technologies into their manufacturing ecosystems, U.S. OSATs can differentiate themselves by focusing on applications tailored to HMLV production, where customization and precision are paramount. For example, deploying AI-driven test solutions for niche markets such as aerospace and defense could establish

U.S. facilities as leaders in high-reliability semiconductor manufacturing.

Government initiatives can support the development of domestic AI capabilities by funding R&D for advanced testing technologies and providing incentives for collaboration with AI-focused startups and research institutions. These efforts can accelerate the deployment of cutting-edge defect detec- tion tools and analytics platforms, ensuring that U.S. OSATs remain at the forefront of technological innovation.

E. Creation of Resilient Testing Solutions

By integrating trained AI models and big data analytics into their testing frameworks, U.S. OSATs can address the increasing complexity of semiconductor packaging while achieving greater efficiency and scalability. These technologies not only reduce operational costs but also enhance supply chain resilience, enabling domestic facilities to compete effectively in a rapidly evolving global market. As the industry continues to push the boundaries of performance, power, and density, AI-driven testing and analytics will be indispensable in ensuring the reliability and competitiveness of advanced semiconductor packages.

VII. Defect Detection Capabilities

A. Advanced Defect Detection in Semiconductor Manufacturing

Advanced defect detection is critical in semiconductor manufacturing due to the increasing complexity and miniaturization of integrated circuits (ICs) [42]. As device geometries shrink, even minor defects can compromise functionality, reliability, and yield, leading to significant financial losses. Advanced defect detection technologies, such as automated X-ray inspection (AXI) [43], automated optical inspection (AOI) [44], scanning electron microscopy (SEM), and deep learning-based approaches, enable early identification of anomalies at nanometer scales, reducing production delays and improving overall process efficiency. Furthermore, leveraging AI for defect detection enhances precision and scalability, addressing challenges in identifying complex defect patterns in multi-layered structures. This proactive approach is essential for meeting stringent quality standards, especially in high-demand sectors like automotive, healthcare, and telecommunications, which rely on defect-free semiconductors for critical applications [45].

B. Techniques for Advanced Defect Detection

1) X-ray Inspection: One of the key benefits of X-ray imaging is its capacity to penetrate multiple layers of material, which enables thorough visualization of internal characteristics without having to disassemble the package. This is especially important in heterogeneous integration, in which components from many technologies and processes are merged into a single package [46]. X-ray imaging is particularly effective at detecting voids, delamination, cracks, solder joint faults, and other structural anomalies that could jeopardize the package's performance and reliability [47]. X-ray imaging technologies, such as high-resolution 3D X-ray microscopy and computed tomography (CT), offer unparalleled insights into package defects [48]. These methods enable the reconstruction of internal structures in three dimensions, facilitating accurate defect localization and analysis. Moreover, the integration of AI further enhances defect detection by automating the identification of anomalies and reducing inspection times.

The study [49], highlights the use of novel 3D X-ray tools capable of achieving sub-micron spatial resolution (down to 0.3 microns). The advanced X-ray imaging techniques allow for non-destructive testing (NDT) across various stages of the packaging process, from intact package inspection to wafer-level analysis. The methods utilized include both high-resolution X-ray microscopy and computed tomography (CT), which enable the reconstruction of three-dimensional models of the internal package structures. This facilitates accurate defect characterization and localization, which are essential for failure analysis and process improvement. Moreover, the versatility of the tools makes them suitable for heterogeneous integration applications, addressing the challenges posed by complex device geometries and interconnects.

In another study [50], the researchers examined various defects in semiconductor devices using X-ray microscopy (XRM), with an emphasis on high-bandwidth memory structures made up of logic and memory dies. The specific defects included voids within solder joints, which are crucial for electrical and mechanical integrity, as well as structural anoma- lies such as irregularities in copper pillars and copper pads. These faults were segmented and analyzed using semantic segmentation models, which enabled the exact identification and characterization of the defective regions. By including these defect categories in the analysis, the study effectively demonstrated the capabilities of XRM paired with sophisticated machine-learning approaches to improve the reliability of defect identification in semiconductor manufacturing. XRM was also employed to analyze various defects such as solder non-wetting, voids, and bump-to-pad misalignments in semiconductor structures, particularly in high-bandwidth memory (HBM) and logic bump samples. By leveraging 3D X-ray microscopy, the authors conducted non-destructive inspections to identify buried structural defects with high resolution [51].

2) Scanning Acoustic Microscopy: SAM is a pivotal technique for detecting and analyzing defects in WLP, particularly in detecting delamination, voids, and cracks within multi-layered structures. SAM operates by emitting high-frequency ultrasonic waves and analyzing the reflected signals to generate detailed acoustic images of the internal structure of a package non-destructively as can be seen in Figure 4.

This non-destructive technique is particularly valuable for inspecting bonded interfaces, such as those in die-attached layers, underfill regions, and RDLs, where mechanical stress or thermal cycling can lead to defects. SAM excels at identi- fying anomalies in areas that are challenging to access using traditional optical inspection methods, making it indispensable for advanced packaging applications.

Moreover, SAM's ability to adapt to varying material prop-

TABLE III
COMPARISON OF ADVANCED DEFECT DETECTION TECHNIQUES

Technique	Defects Detected	Advantages	Limitations
X-Ray Microscopy (XRM)	Voids, cracks, delamination	Non-destructive, high-resolution, suitable for multilayer inspection	High equipment cost
Scanning Acoustic Microscopy (SAM)	Delamination, cracks	Ideal for bonded interfaces, effective for subsurface defects	Limited to certain materials
Scanning Electron Microscopy (SEM)	Surface contamination, micro-cracks	High magnification, nanometer-scale precision, elemental analysis	Requires specialized sample preparation

erties and package geometries enhances its versatility. By utilizing multiple modes, such as A-scan (amplitude), B-scan (cross-sectional imaging), and C-scan (planar imaging), SAM provides comprehensive insights into both surface and subsurface features. These capabilities make it a critical tool for maintaining the integrity and performance of wafer-level packages in high-reliability applications like automotive and aerospace sectors.

Incorporating SAM into quality assurance workflows ensures that defects are identified at early stages of production, reducing the risk of failures and improving overall manufacturing yield. As WLP continues to advance, the role of SAM in ensuring defect-free production will only grow, solidifying its importance in the semiconductor industry.

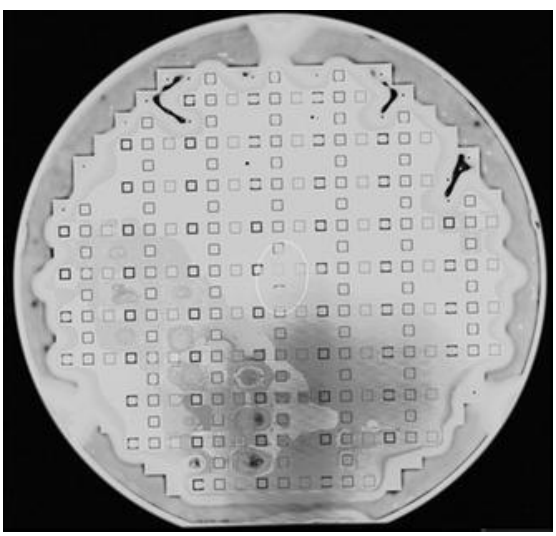

Fig. 4. Non-destructive wafer-level bond defect identification by scanning acoustic microscopy [52].

3) Scanning Electron Microscopy (SEM): SEM is an essential tool for defect detection in WLP. It offers high-resolution imaging and analysis of surface and subsurface structures. SEM uses a focused beam of electrons to scan a sample, generating detailed images that reveal surface topography, material composition, and structural features with nanometer- scale precision.

In WLP, SEM is particularly effective in identifying defects such as cracks, voids, and contamination on fine interconnects, bumps, and RDLs. Its high magnification capability allows for the inspection of intricate patterns and geometries beyond the resolution of optical inspection techniques as depicted in Figure 5. This makes SEM indispensable for analyzing advanced packaging technologies like 3D stacked devices.

Furthermore, advanced SEM techniques, such as energy-dispersive X-ray spectroscopy (EDS), extend its utility by enabling elemental analysis of defects [53]. This is espe- cially useful for identifying contamination or material inconsistencies that could compromise the package's reliability. Secondary electron imaging (SEI) and backscattered electron imaging (BEI) modes further enhance defect detection by providing contrast variations based on material density and surface morphology.

SEM's role in WLP is seen in Figure 5. extends beyond defect detection to process optimization and failure analysis. By providing detailed feedback on manufacturing processes, SEM helps engineers refine etching, deposition, and planarization steps, ensuring higher yield and quality. As the industry pushes toward smaller nodes and more complex designs, SEM remains a cornerstone technology for achieving defect-free semiconductor packaging and meeting the rigorous demands of sectors like consumer electronics, automotive, and telecommunications.

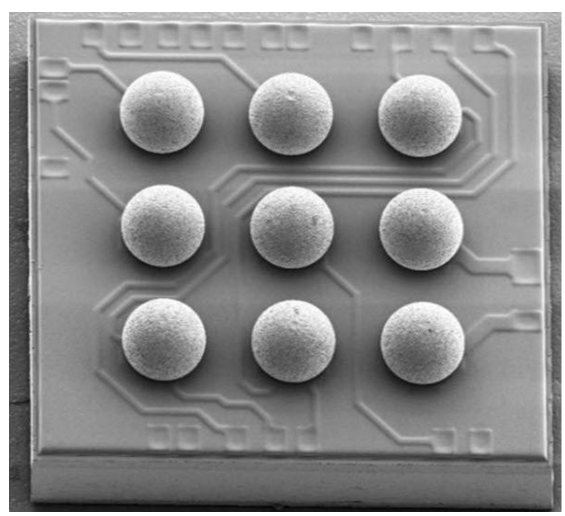

Fig. 5. SEM Image of WLP [54]

C. *OSAT Facilities in Defect Detection Innovation*

OSAT facilities play a critical role in advancing defect detection methodologies, particularly in WLP. As the demand for high-performance, miniaturized devices grows, OSATs are tasked with implementing and innovating cutting-edge inspection technologies to ensure quality and reliability while maintaining competitive production costs. Table III compares advanced defect detection techniques, showcasing their specific advantages, limitations, and the types of defects they address.

One of OSATs' primary contributions to defect detection innovation is their ability to integrate state-of-the-art inspection tools such as automated optical inspection (AOI), automated X-ray inspection (AXI), and SEM into high-volume manufacturing environments. These facilities continuously enhance the capabilities of these tools by collaborating with equipment manufacturers to develop customized solutions tailored to address specific challenges in advanced packaging, such as the detection of defects in fine-pitch interconnects, RDLs, and TSVs.

Moreover, OSATs are driving the adoption of AI and machine learning (ML) in defect detection. By leveraging these technologies, OSAT facilities can analyze vast amounts of inspection data to identify complex defect patterns and predict potential failure modes. This proactive approach not only reduces production delays but also improves yield and reliability, which are critical in industries such as automotive, telecommunications, and healthcare.

In addition to technological advancements, OSATs foster innovation by providing a collaborative platform for ecosystem partners, including foundries, equipment manufacturers, and research institutions. By sharing expertise and resources, these partnerships accelerate the development and deployment of novel defect detection methodologies, such as hybrid inspection systems that combine multiple techniques to achieve higher sensitivity and accuracy.

Finally, OSAT facilities play a strategic role in standardizing defect detection practices across the semiconductor industry. Their focus on quality assurance and reliability testing ensures that the latest innovations are robust, scalable, and aligned with industry standards. This not only enhances the overall manufacturing ecosystem but also builds trust among end-users who rely on defect-free semiconductor packages for critical applications.

Through their commitment to continuous improvement and collaboration, OSATs remain at the forefront of defect detection innovation, enabling the semiconductor industry to meet the challenges of modern packaging technologies and deliver exceptional quality and performance products.

VIII. Strategic Path Forward for the U.S Semiconductor Industry

A. *Government Support for Foundry 2.0 and OSAT's*

The transition to Foundry 2.0 and the growth of OSAT facilities necessitate substantial infrastructure investments and strategic planning to keep pace with advancements in semiconductor technology. While the U.S. government semiconductor policies are pivotal in bolstering domestic capabilities, similar initiatives are gaining momentum globally. For instance, Europe's "European Chips Act" focuses on strengthening regional manufacturing and supply chain resilience [55], while South Korea's K-Semiconductor Strategy and Taiwan's continuous investments in advanced packaging have solidified their global leadership [56].

These global efforts highlight the importance of international collaboration and regional specialization in advanced packaging and WLP. For example, the European Chips Act provides funding for research into next-generation packaging technologies and promotes cross-border partnerships among member states [57]. Similarly, Asian countries emphasize advanced packaging solutions like 2.5D and 3D integra- tion to maintain their competitive edge. By leveraging such government-backed initiatives, OSAT facilities worldwide can align with Foundry 2.0's emphasis on cutting-edge packaging and testing solutions, ensuring that they meet the increasing demand for high-performance semiconductor devices.

These global policies collectively aim to reduce dependency on any single region, ensuring a diversified and resilient semiconductor ecosystem. For instance, Japan's revitalization efforts in semiconductor manufacturing through public-private partnerships focus on niche areas like materials innovation, complementing other global efforts in advanced packaging [58]. By aligning these policies with industry-wide goals, governments, and companies can foster an interconnected ecosystem capable of addressing geopolitical tensions and supply chain disruptions.

B. *Industry Partnership and Collaborative Efforts*

In an increasingly interconnected semiconductor landscape, strategic global partnerships have become vital for fostering innovation and sustaining competitiveness. The Foundry 2.0 model and the growth of OSAT facilities depend on collaborations that transcend borders. Key players like TSMC, Samsung, and Intel have invested in cross-regional alliances to expand capabilities in assembly, packaging, and testing. Such partnerships enable OSAT facilities to share best practices, pool resources, and accelerate technological advancements.

One noteworthy example is the collaboration between Taiwanese OSAT companies such as ASE, Powertech Technology Inc. (PTI), and King Yuan Electronics Corp. (KYEC), and European design houses like SiPearl, STMicroelectronics, NXP Semiconductors, Dolphin Design, and Pragmatic Semiconductor to develop next-generation chiplet architectures [59]. These partnerships leverage Taiwan's expertise in advanced packaging, such as 2.5D/3D integration and chiplet-based solutions, alongside Europe's focus on innovative chip designs, to create robust and scalable solutions [60]. Similarly, South Korean OSAT companies, including Hana Micron, Nepes Corporation, and LB Semicon, work closely with U.S. fabless companies such as Qualcomm, NVIDIA, and AMD to optimize WLP processes [61].

These collaborations combine south korea's advanced testing and packaging capabilities with the U.S.'s leadership in semiconductor design, ensuring a faster time-to-market for new products.

Joint research initiatives and shared investments have proven instrumental in addressing the high cost of developing new technologies. Global consortia, such as the International Semiconductor Manufacturing Initiative (ISMI), facilitate knowledge exchange and collaborative problem-solving. These efforts are particularly impactful in overcoming challenges like thermal management, power efficiency, and miniaturization, which require multidisciplinary expertise.

By fostering such collaborations, the semiconductor industry can create a resilient supply chain network, ensuring that OSAT facilities in the U.S. remain agile and adaptive to emerging technological demands. This interconnected approach strengthens the industry's ability to innovate, meet diverse market needs, and mitigate risks posed by regional disruptions.

IX. Global Insights to Local Action

A. Government Support

The U.S. government's support represents a historic opportunity for U.S. OSAT facilities to modernize their capabilities and bridge the gap with global leaders. To make the most of this initiative, investments must be directed toward cutting-edge infrastructure tailored for advanced packaging processes such as 2.5D and 3D integration, as well as high-density interconnect technologies. Beyond infrastructure, fostering a robust pipeline of skilled engineers and technicians will be critical. By aligning these investments with key emerging areas, U.S. OSATs can position themselves to support the demands of AI, high-performance computing, and other next- generation applications. These steps not only strengthen the domestic semiconductor industry but also create a competitive edge that offsets labor and cost disadvantages relative to Asia.

B. Advanced Packaging Innovations

Taiwan's success in heterogeneous integration and South Korea's leadership in high-bandwidth memory (HBM) technologies illustrate the impact of concentrated R&D efforts. For U.S. OSATs, adapting these global best practices requires establishing collaborative research hubs that focus on addressing unique technical challenges such as interconnect density, thermal management, and yield optimization in WLP. These hubs, supported by academia, industry, and government, could act as innovation centers for developing modular, scalable packaging solutions. By focusing on R&D that emphasizes agility and niche market applications—such as automotive and aerospace semiconductors U.S. OSATs can redefine their role in the global semiconductor supply chain.

C. Integrated Ecosystems with Domestic Partners

Historically, isolated operations have limited the effectiveness of U.S. semiconductor manufacturing. To remain competitive, U.S. OSATs must adopt a more collaborative model that mirrors the integrated ecosystems of Asia. Strong partnerships with domestic IDMs and fabless companies are essential to ensuring that packaging innovations align seamlessly with upstream designs and downstream market needs. Such partnerships can be bolstered through co-development agreements, where OSATs work directly with IDMs to incorporate advanced packaging processes into product roadmaps. For example, partnerships with Qualcomm and NVIDIA could yield tailored solutions for AI and high-performance comput- ing applications, reducing time to market and strengthening the domestic ecosystem. This approach mitigates reliance on foreign supply chains and builds a self-sufficient, resilient U.S. semiconductor industry.

D. AI and Big Data for Competitive Advantages

The adoption of AI and big data analytics presents a transformative opportunity for U.S. OSATs. Global leaders such as South Korea have integrated AI into manufacturing processes to optimize defect detection and improve yield rates. U.S. OSATs can lead in this area by developing proprietary AI-driven models for advanced inspection methods, including X-ray imaging and scanning electron microscopy (SEM). These technologies not only enhance manufacturing efficiency but also reduce operational costs, helping U.S. OSATs remain competitive despite higher labor expenses. By integrating AI across all stages of packaging and testing, domestic OSATs can achieve higher precision and scalability, aligning their processes with the demands of Foundry 2.0.

E. Adaptation of Global Best Practices

Rather than attempting to replicate foreign models outright, U.S. OSATs should adopt global best practices to address their unique challenges and opportunities. By focusing on automation and AI to offset higher operational costs, prioritizing modular and flexible facility designs, and targeting sectors like aerospace and defense where the U.S. has a natural competitive edge, domestic OSATs can create a differentiated value proposition. Regional specialization, bolstered by government support and collaborative partnerships, ensures a sustainable pathway to reducing reliance on foreign supply chains and building a robust semiconductor ecosystem.

Conclusion

The U.S. OSAT sector is at a critical inflection point, with the opportunity to establish itself as a key contributor to the global semiconductor industry. Meeting the growing demands of advanced applications such as artificial intelligence, 5G, and high-performance computing requires a clear and actionable roadmap focused on technological advancement, ecosystem collaboration, and supply chain resilience. Supported by strategic initiatives like the CHIPS and Science Act, U.S. OSATs are well-positioned to close the competitive gap with global leaders.

To achieve this, U.S. OSATs must prioritize investments in state-of-the-art packaging technologies, including 2.5D/3D integration, WLP, and chiplet architectures. These advancements are essential to addressing the power, performance, and density requirements of modern semiconductor designs. Equally critical is the integration of AI-driven test solutions and big data analytics into testing frameworks. These methodologies enable greater precision in defect detection, process optimization, and yield improvement, ensuring that U.S. OSATs can maintain efficiency and scalability in increasingly complex manufacturing environments.

Collaboration is a fundamental pillar of this strategy. Strengthening partnerships with IDMs, fabless companies, and academic institutions will ensure that packaging and testing innovations align with upstream design requirements and downstream market demands. Such collaborations also facilitate knowledge exchange and accelerate the deployment of next-generation packaging solutions. Furthermore, localized supply chains must be developed to mitigate risks associated with foreign dependencies, enhancing the resilience of the domestic semiconductor ecosystem.

By aligning investments, technological innovation, and strategic collaborations, U.S. OSATs can enhance their global competitiveness while contributing to a more secure and sustainable semiconductor supply chain. This roadmap provides a pathway for U.S. OSATs to redefine their role in the semiconductor landscape and ensure long-term relevance in a rapidly evolving industry.

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