FOUR DIMENSIONS OF HETEROGENEOUS INTEGRATION

Definitions

Heterogeneous: made up of dissimilar or diverse parts

Integration: combining different things to form a unified whole

Heterogeneous Integration: combining dissimilar or diverse parts to form a unified whole

Introduction

The brilliance of the integrated circuit (IC) is that its components – transistors, resistors, capacitors, wiring – are all built into a single piece of material. Its enormous advantages in speed, power, and miniaturization have propelled the electronics industry into every corner of modern life.

The System-on-Chip (SoC) model is an extension of the IC. An entire set of ICs is redesigned to be built onto a single piece of material. This solution further reduces footprint and power usage; it has become the industry standard for complex broad-use applications.

Advanced Packaging (AP) also brings together an entire set of ICs into a single integrated device. Unlike the monolithic SoC model, it does not build everything on a single piece of material. Instead, it integrates components that are built separately. This allows *heterogeneous integration* at several levels.

Four Types of Heterogeneity

1. Wafer Processing Recipes

Components are built onto semiconductor wafers in a complex multi-step process. Precise modifications in the various process steps influence the characteristics of that wafer. The process recipes are unique, nuanced, and proprietary, but they fall into a few general categories:

a) **High Performance**
Optimized for speed, these recipes build fast transistors for logic and processing. The downside is that the chips consume extra power and suffer from high leakage. A memory chip built in this process would draw unsustainable amounts of power.

b) **Low Power**
These recipes use minimal power and provide low leakage. The tradeoff is speed.

c) **Memory**
Memory, always a critical element, has very specific requirements. Recipes that are tightly

focused on memory come at the expense of anything else. For example, DRAM processes push leakage to near-zero levels; logic built in a DRAM process would be impossibly slow.

d) **General Purpose**
If a chip contains a little of everything – some memory, some computation, some analog features – these balanced recipes provide a workable compromise.

A single-purpose IC can be built in whichever process best suits its needs. An SoC, however, is forced to make compromises among all its functions. Advanced Packaging (AP) allows each component to be built in its best process and then integrated into one highly optimized device.

➢➢ ***THAT'S HETEROGENEOUS INTEGRATION OF DIFFERENT PROCESS RECIPES.***

This was probably the first type of heterogeneous integration to be successfully exploited in the AP ecosystem. Stacking technology is not affected at all by the recipes used to create the individual layers.

2. Process Nodes

A "process node," also known as a "technology node," defines the smallest features that a manufacturing technology can create on a wafer. Process nodes became smaller and smaller over the years as semiconductor technology advanced. In the 1960s the typical node was 50 microns; from 1984 to 2022 the leading-edge node decreased from one micron to three nanometers.

Smaller nodes occupy less space, build faster transistors, and are more power-efficient. The smallest nodes are therefore the best choice for processors and other transistor-heavy designs. However, older nodes have their own advantages: they are more stable, less expensive, and can be fabricated on smaller wafers. ICs built in these "legacy" nodes can handle higher voltages and are better for precision analog applications that require tight measurement: microphone amplifiers, A/D converters, etc.

An SoC, being built all at once, can use only one node; a device built with Advanced Packaging (AP) can incorporate components built at different nodes, each in the node best suited for its function.

➢➢ ***THAT'S HETEROGENEOUS INTEGRATION OF DIFFERENT PROCESS NODES.***

AP easily accommodates different nodes; metal layers do the translation from one geometric scale to another.

3. Materials

In common parlance, silicon is nearly synonymous with semiconductors. Silicon is abundant, easy to use, and unrivaled in its support for high-density, low-power components. However, there are other semiconductor substrate materials that outperform silicon in niche applications. For example:

Lithium niobate (LiNbO3) is a hard, transparent, ferroelectric, piezoelectric, electro-optic material, ideal for photonics, acoustic wave guides, etc.

Gallium nitride (GaN) provides high power density, frequency, and efficiency; it's good for optoelectronics.

Indium phosphide (InP) can both conduct and produce light. It's excellent for high frequency, radio frequency, high-speed electronics; optoelectronics; and photovoltaics.

Silicon carbide (SiC) is nearly as hard as diamond and exhibits high thermal conductivity, thermal shock resistance, and resistance to oxidation at high temperatures. It's used in power converters, LEDs, and detectors.

Gallium antimonide (GaSb) has properties useful for infrared detection, including long cutoff wavelengths. It is used in infrared cameras and sensors.

Obviously, an SoC is built on just one material. Advanced packaging can integrate components made of dissimilar materials.

➢➢ ***THAT'S HETEROGENEOUS INTEGRATION OF DIFFERENT MATERIALS.***

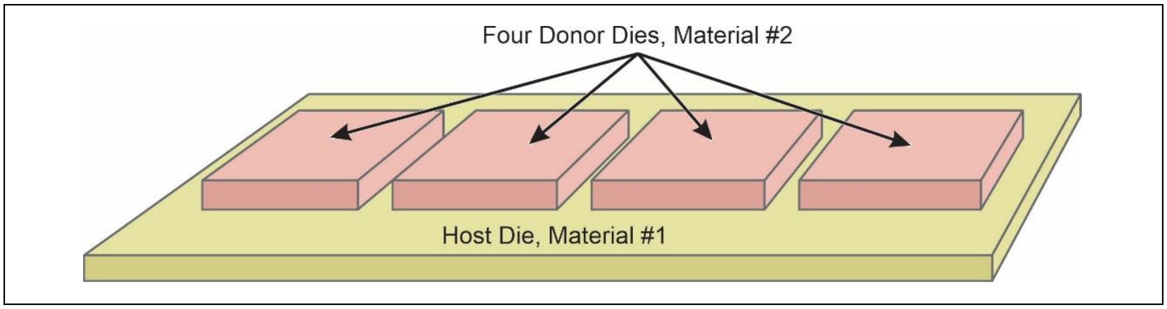

Figure 1: Dies made of different materials, 3D integration

This one is not easy! Some specialty materials are available only on very small wafers, which require specialized equipment. Brittle, fragile materials demand extra-careful handling. And, in all cases, different materials have different coefficients of thermal expansion (CTE). Without proper engineering, CTE mismatch can cause warpage, delamination, or even breakage. This is a formidable challenge for Advanced Packaging – nonetheless, skilled and artful engineering can achieve reliable success. Process engineers continually invent and refine their recipes; AP will undoubtedly expand to encompass a wider set of materials.

Real world applications at NHanced:

- ***Photonic transceiver for a large commercial telecommunications company***

  Multiple pieces of thin film lithium niobate (TFLN) are 3D integrated via hybrid bonding with a silicon host die. Each TFLN acts as an optical modulator.

- ***Infrared (IR) sensor for many different US Government applications***

  A gallium antimonide (GaSb) detector is 3D integrated via hybrid bonding with a silicon CMOS readout integrated circuit (ROIC).

4. Sources (Manufacturers/Vendors)

Some manufacturers make top-of-the-line memories; others make superlative processors. Niche companies specialize in accelerometers, optoelectronics, energy harvesting, wireless communications, etc. The ideal Advanced Package would contain the best of the best, regardless of vendor, integrated into one extraordinary device.

➤➤ ***THAT'S HETEROGENEOUS INTEGRATION OF DIFFERENT SOURCES.***

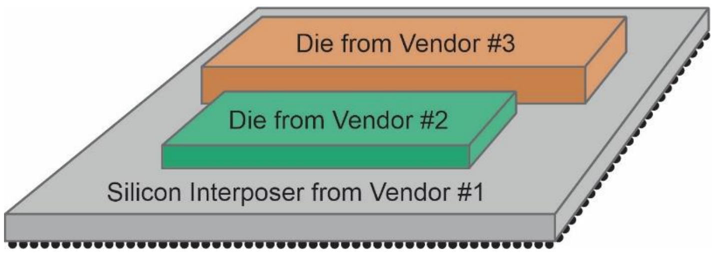

Figure 2: Dies from different sources, 2.5D integration

Like mixing materials, using dies from different manufacturers is tricky. The manufacturers may use different test processes, different scribe lanes, different operating voltages – the packaging needs to accommodate all of this.

Beyond the technical complexities, there is the problem of business negotiations. Not every manufacturer is willing to sell its components as bare dies. On top of that, integrating a bare die requires intimate knowledge of all its specifications. That is proprietary information; it demands mutual trust and a solid legal NDA.

When the chiplet paradigm gains enough traction, integrating chiplets from different sources should get a lot easier. For now, it remains in the hands of those companies who maintain firm, tested relationships with a range of suppliers.

Real world application at NHanced:

- ***ASIC for a US Government prime contractor***

  A custom-designed die (manufactured by GlobalFoundries) is 2.5D integrated via hybrid bonding onto an interposer (manufactured by NHanced) along with an FPGA die (manufactured by a commercial vendor).

Conclusion

Heterogeneous integration mixes processes, nodes, materials, and sources that cannot be combined on a monolithic device. Advanced Packaging uses heterogeneous integration to leverage best-in-class components into outstanding new devices. Some techniques are quite challenging and demand considerable expertise; nonetheless, successful applications are already delivering results. The scope of credible applications will continue to widen as new material handling processes are developed and as a commercial chiplet ecosystem begins to emerge.