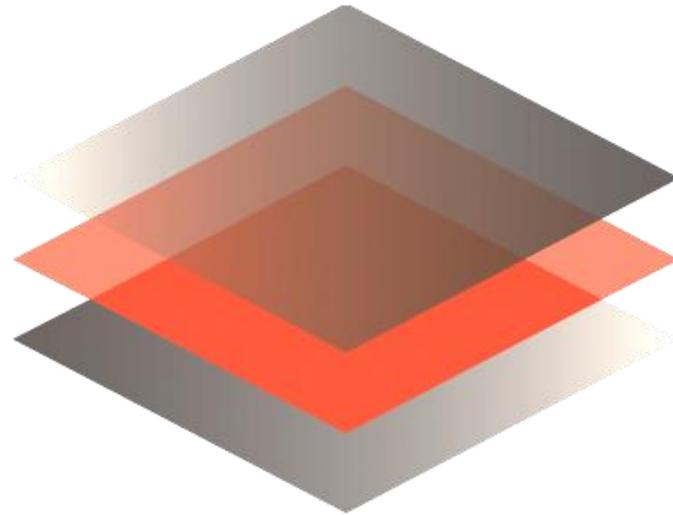


# NHanced Semiconductors



Aug 1, 2024

Robert Patti

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630-561-6813



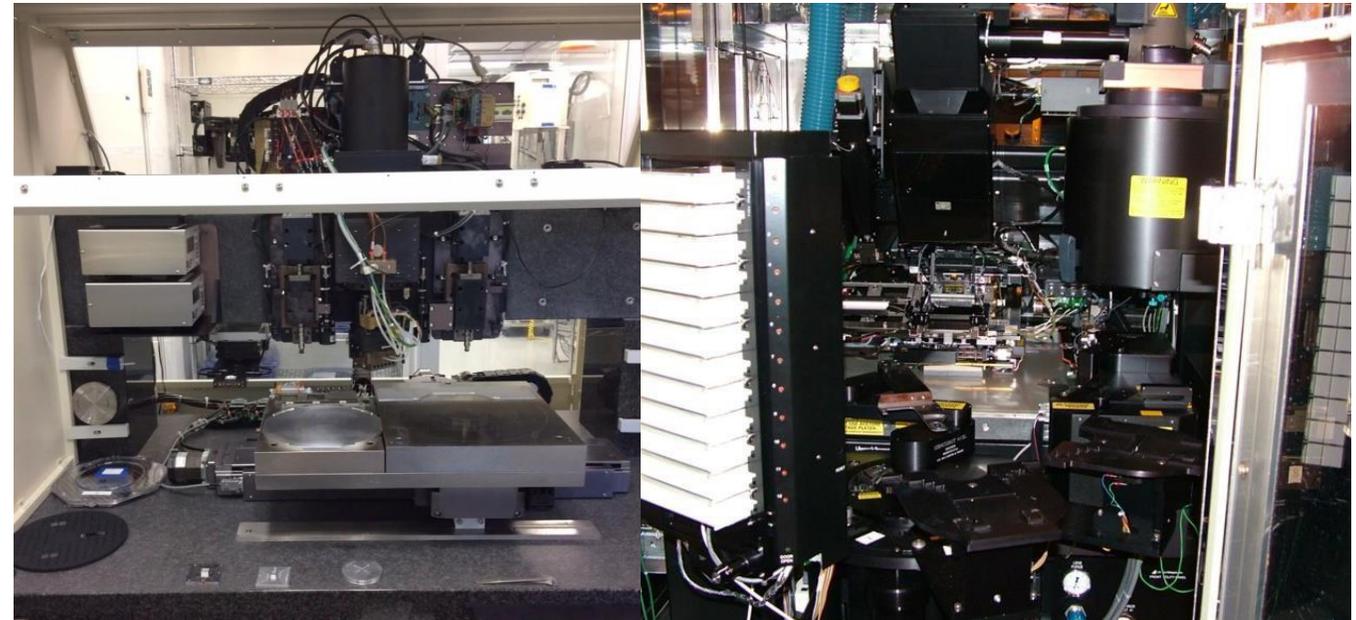
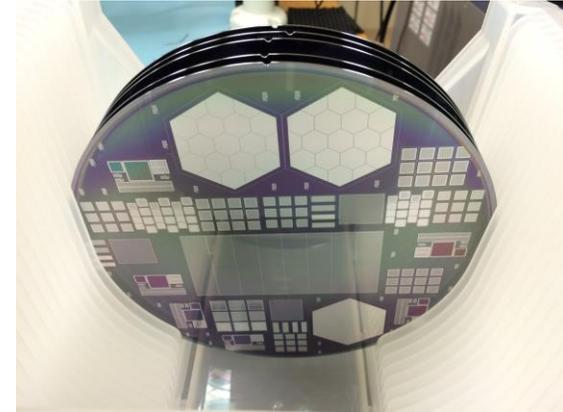
# NHanced Background

- We target specialty niche markets with Advanced Packaging, Additive Manufacturing, and specialty BEOI:
  - Photonics
  - Fluidics
  - True Heterogenous Integration
  - RadHard
  - Quantum devices
  - FPGAs
  - Memory including ReRAM, MRAM, FeRAM, EEPROM, DRAM, SRAM
  - AI/ML/Exascale
  - RFID
  - Medical
  - Down-hole to deep-cryo
- Mixed commercial and A&D customers and production
- 80 employees
  - Deep technical bench with industry recognized experts on staff.
  - Core team has worked together for >20 years
  - Industry awards for advanced packaging
- Tightly held US ownership



# NHanced Semiconductors

- Batavia, IL: Design and Test
  - Complete front end and back end design down to 12nm
  - Supports AI and HPC systems development
- Morrisville, NC: Foundry 1
  - 50mm to 200mm wafers
  - Copper, Al, Ni BEOI
  - Interposers
  - 2.5/3D Integration
  - W2W, D2W
- Morrisville, NC: Foundry 2&3
  - HVM AP 200mm 2025
  - HVM AP 300mm 2026
- Odon, IN: Packaging
  - Packaging
  - RadHard Microelectronics
- Odon, IN: Interposer Foundry 4
  - HVM 1.5M/yr
  - In buildout – 1Q2025 start



# New Tools and Capabilities - Highlights

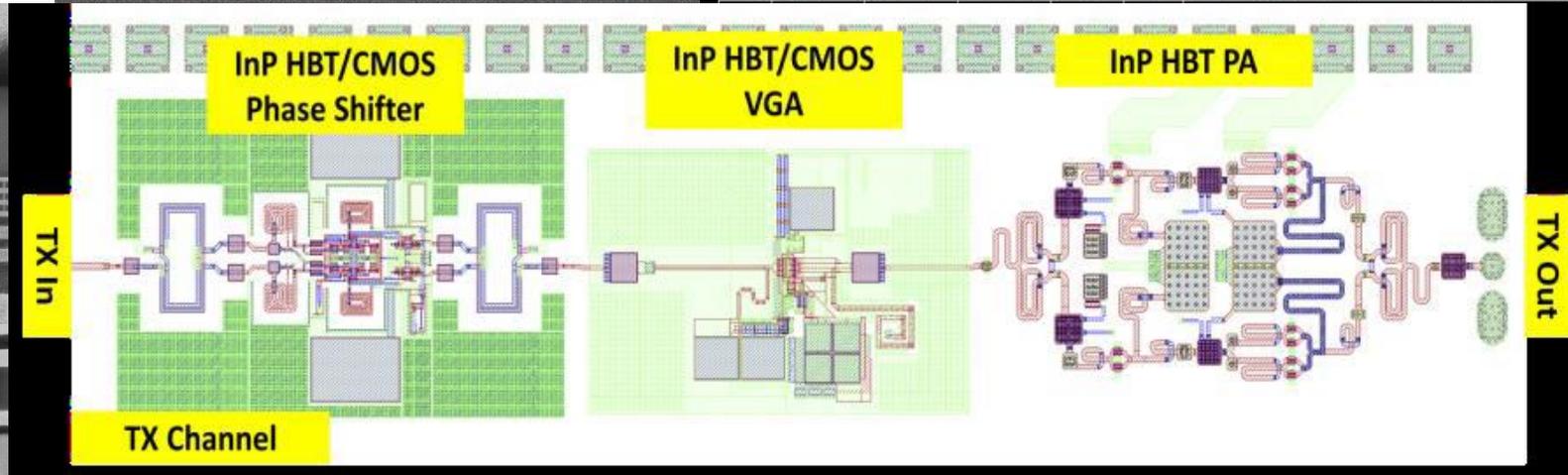
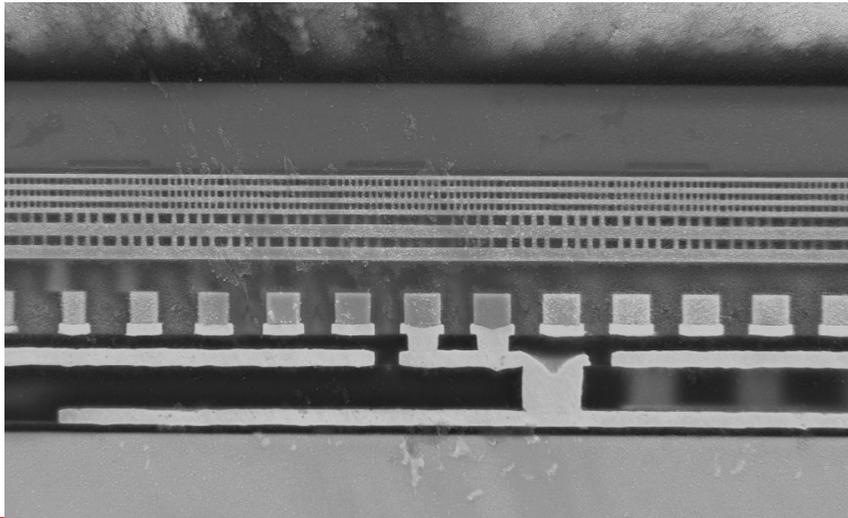
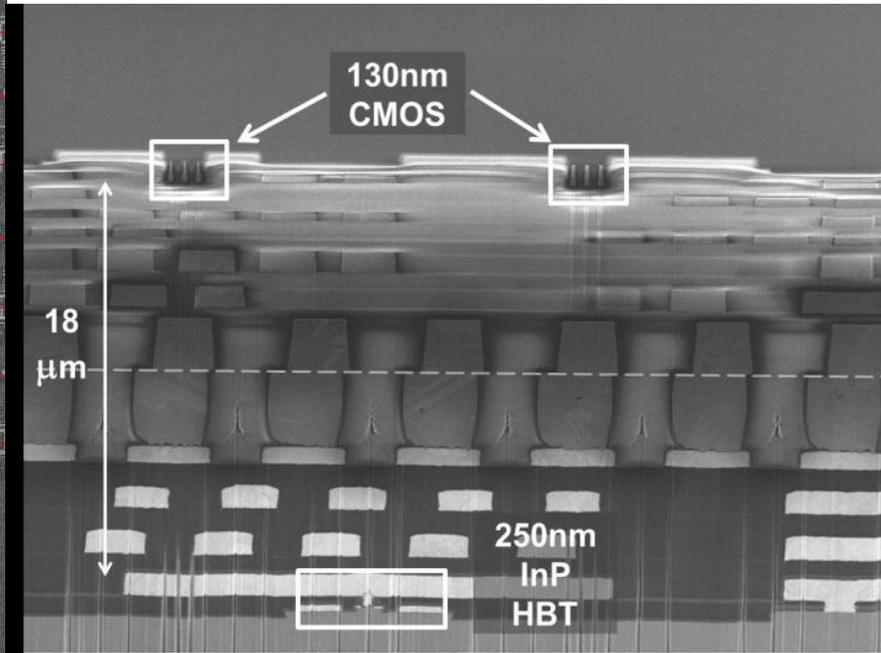
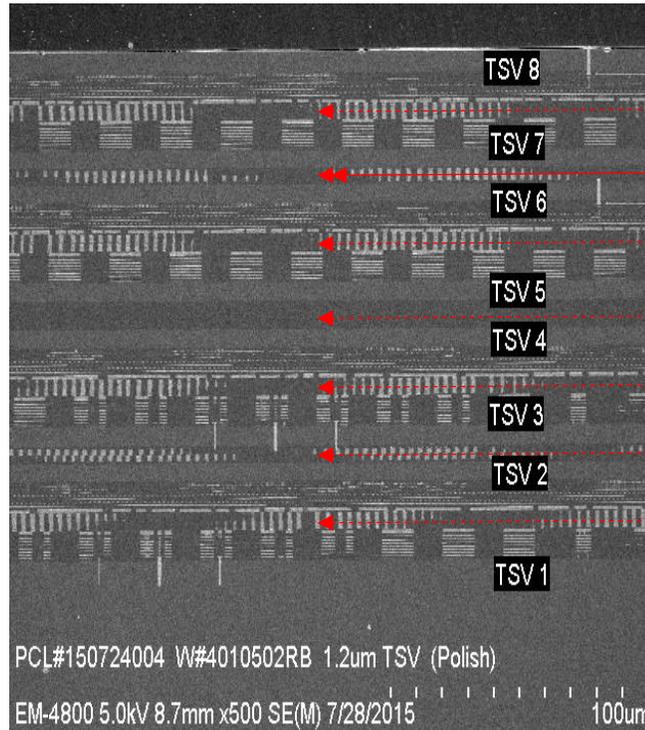
- Die to Wafer Bonder
  - Besi Next Gen
  - Better than 200nm accuracy
  - >2k die per hour
  - >three 9s going to five 9s
- Bosch Etch
  - PlasmaTherm
- Oxide/Nitride
  - Trion
  - Low temperature – down to 70C oxides
  - Stress balanced
- Pd/Au Plating
  - Quantum device enablement
- Large TSV Fill
  - 50x300um, 25x200um
- New Oxide Etch
  - AMAT P5000
- New PVD
  - Endura 5500
- New Metrology
  - Next gen ultrasound
- New Production Plater
  - Raider
- New ALD
  - Arradance
  - High aspect ratio TSV barrier and seed
  - High k thin films
- I-Line 1x litho
  - NXQ8000
  - Full wafer reticle – stitchless interposers to full wafer size
  - Near I-line stepper performance: 1um L/S
  - Through wafer IR alignment



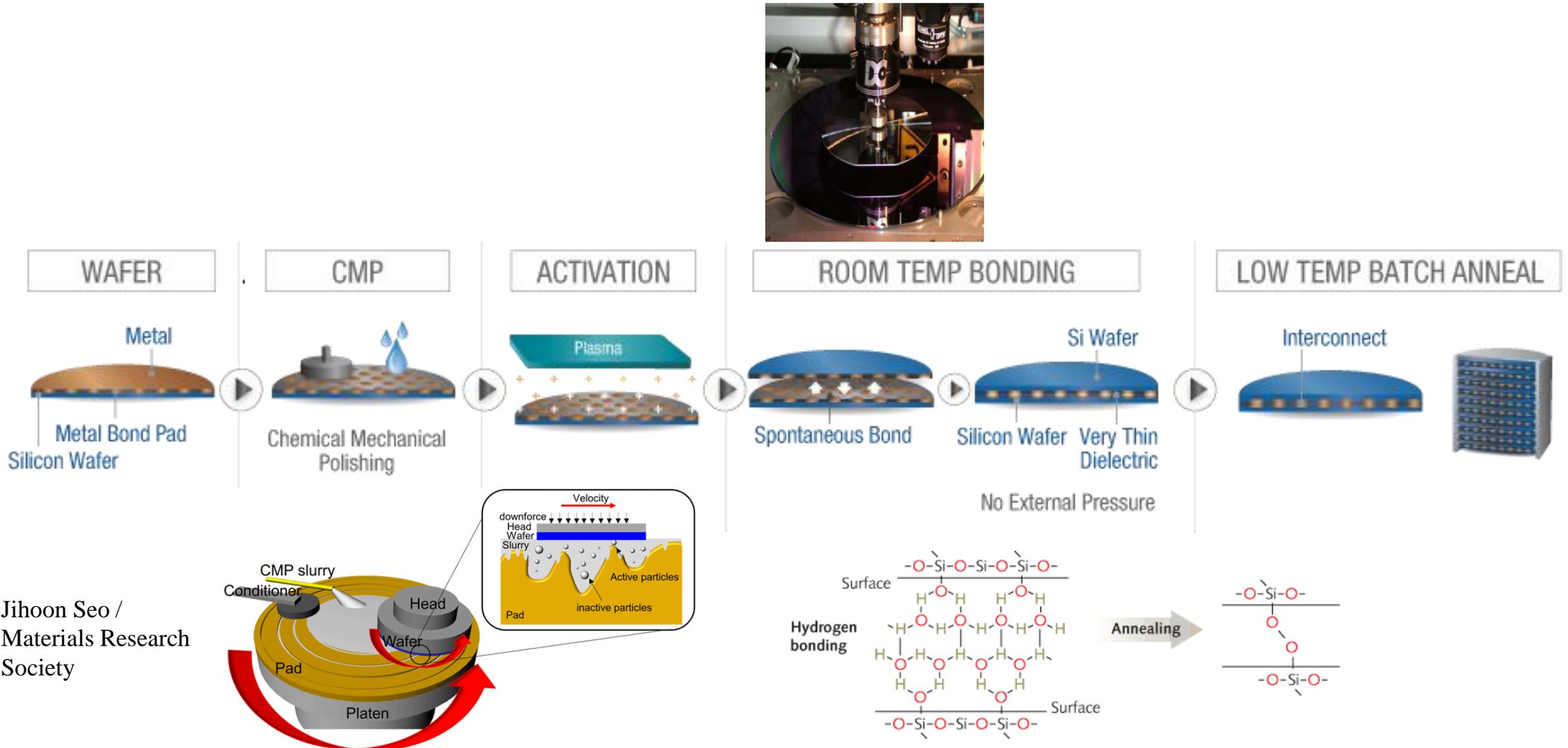
# AP Services: Bonding

- High maturity
- Up to 20 tiers
- True heterogenous with micron scale interconnects
- Die-to-wafer, wafer-to-wafer

Mixed Materials  
Best of Class

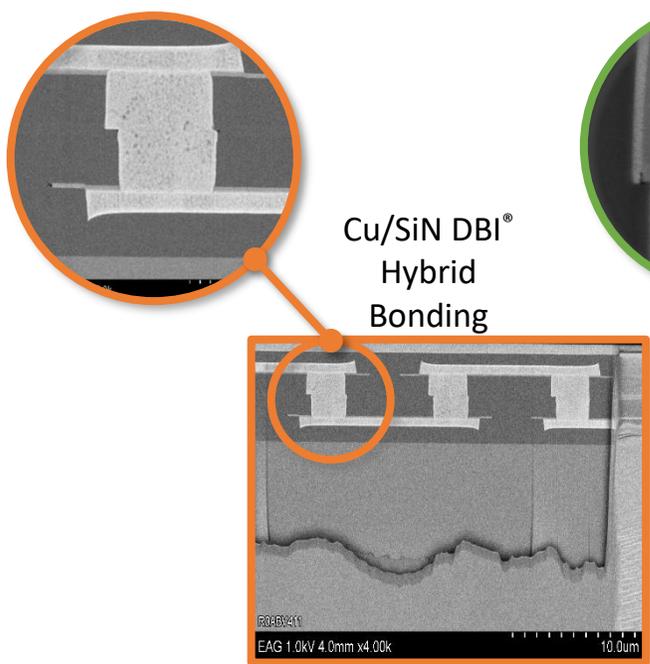


# DBI<sup>®</sup>: Low Temperature Hybrid Bonding Process



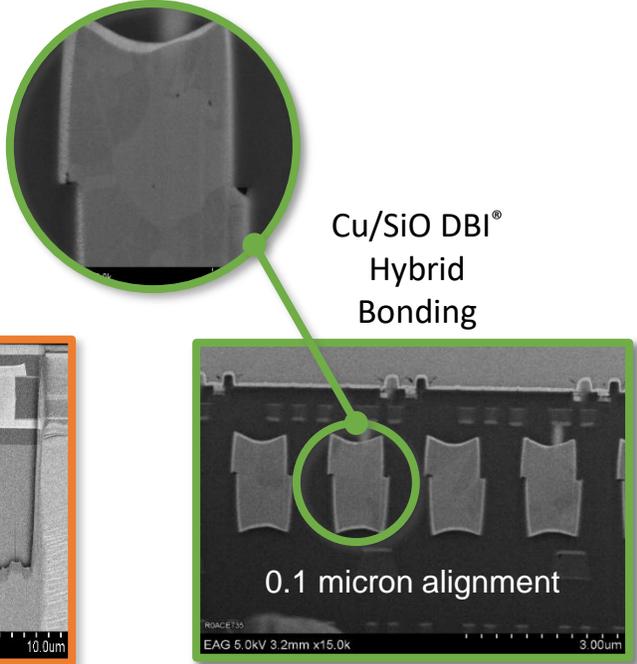
Jihoon Seo /  
Materials Research  
Society

# Hybrid Bonding Interconnect Pitch Scaling



Cu/SiN DBI<sup>®</sup>  
Hybrid  
Bonding

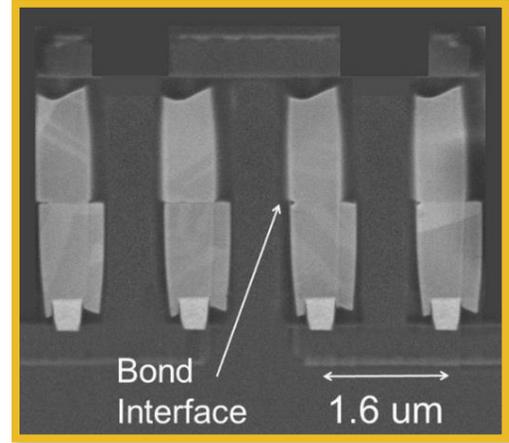
10 µm DBI<sup>®</sup> pitch, 300°C



Cu/SiO DBI<sup>®</sup>  
Hybrid  
Bonding

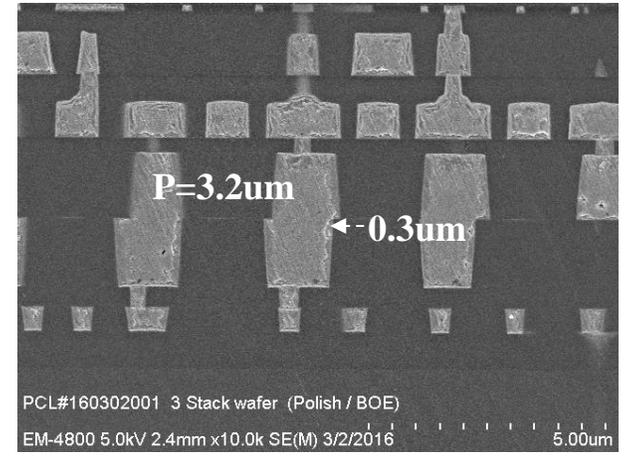
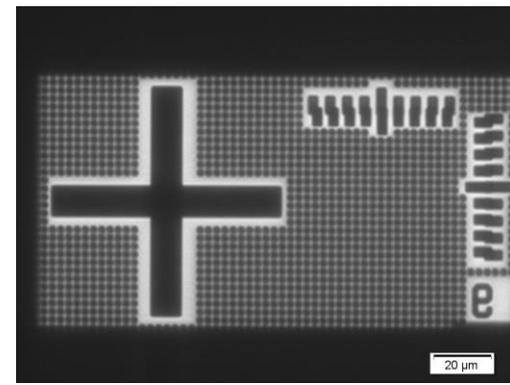
1.9 µm DBI<sup>®</sup> pitch, 300°C  
0.1 micron alignment

Scalable To < 1µm Pitch  
0.8µm Pitch Demonstrated



1.6 µm DBI<sup>®</sup> pitch,  
300°C

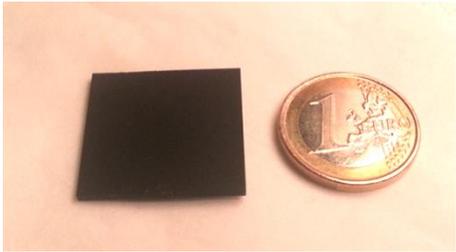
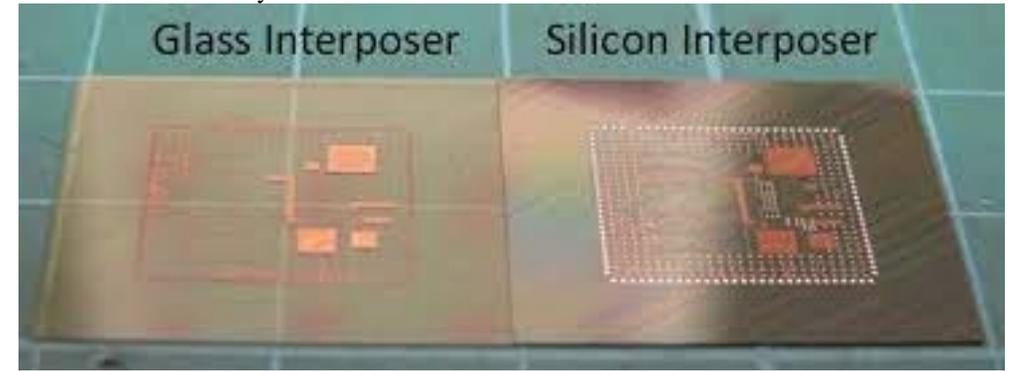
- WtoW 3sigma < ±1µm misalign performance
- DtoW 3sigma < ±200nm misalign performance
- Production Minimum pitch = 2.44µm



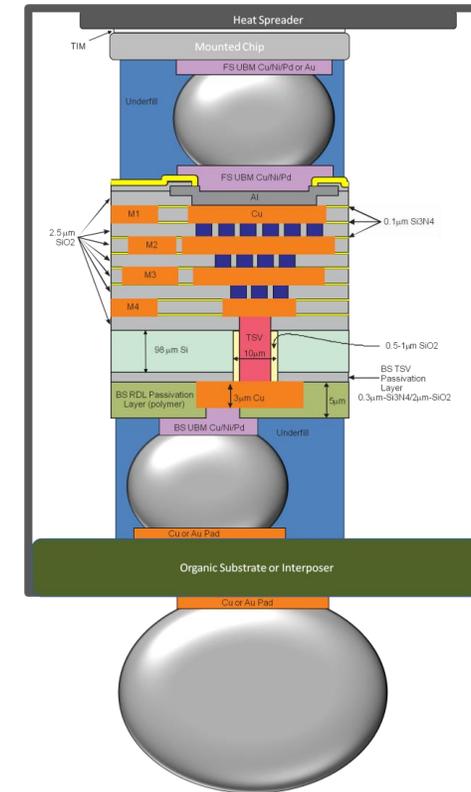
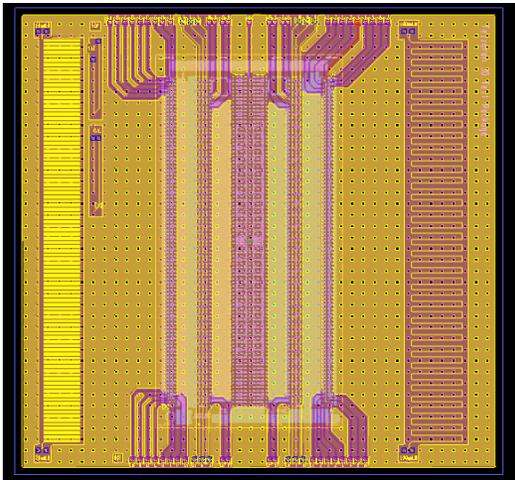
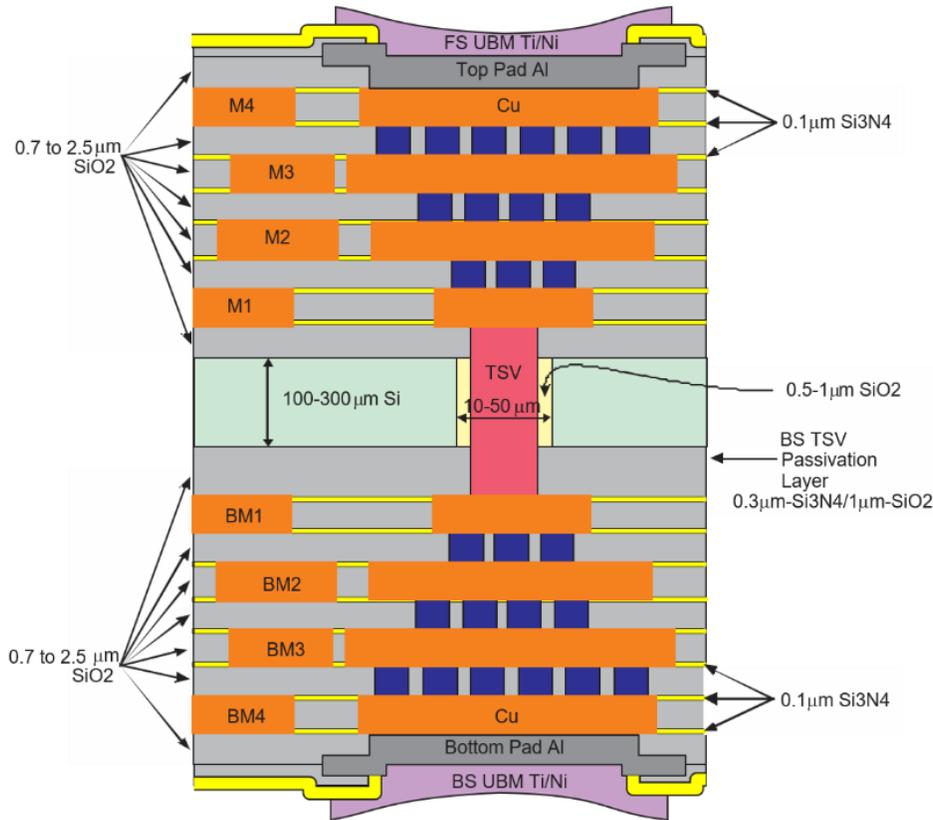
# AP Services: Interposers

- Up to full wafer scale
- HP 2um thick wiring is standard

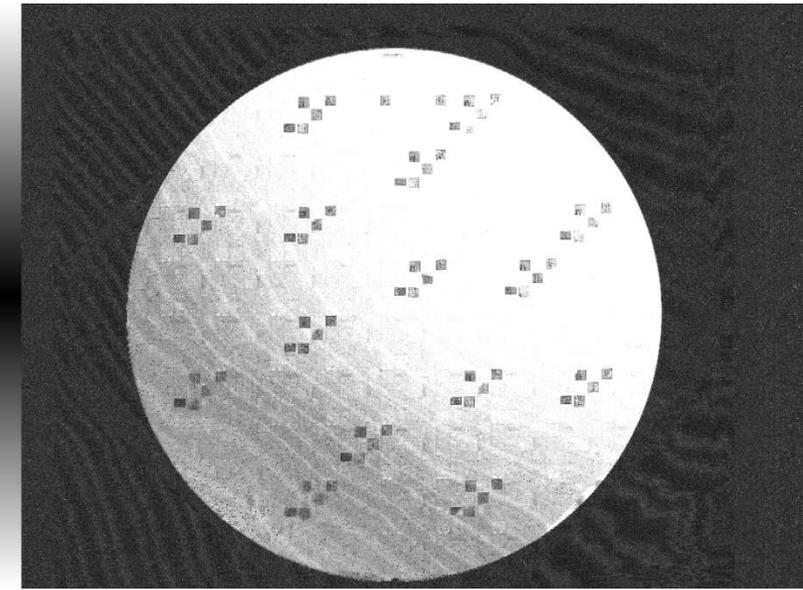
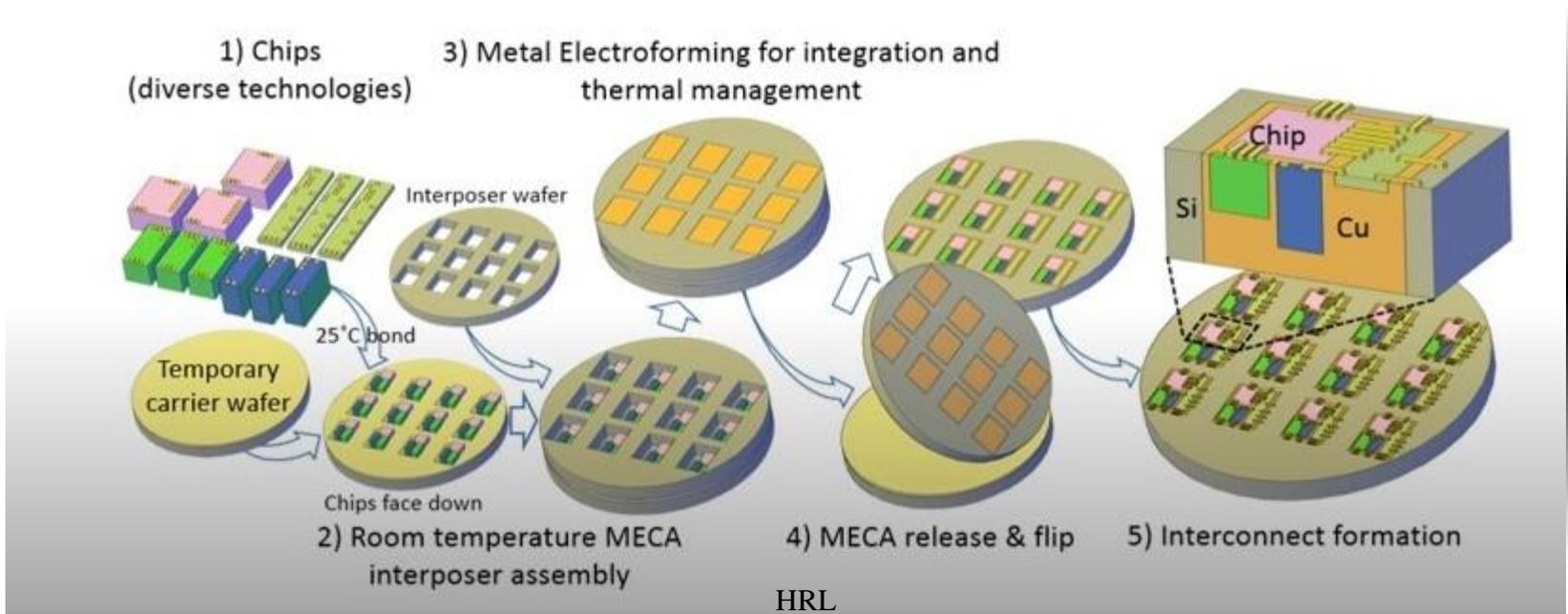
Mosaic Microsystems



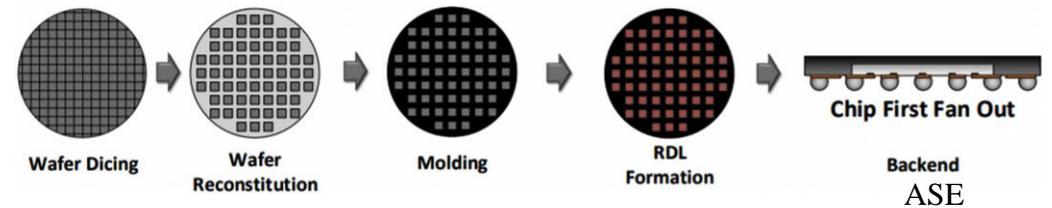
Up to 8 layers of wiring available



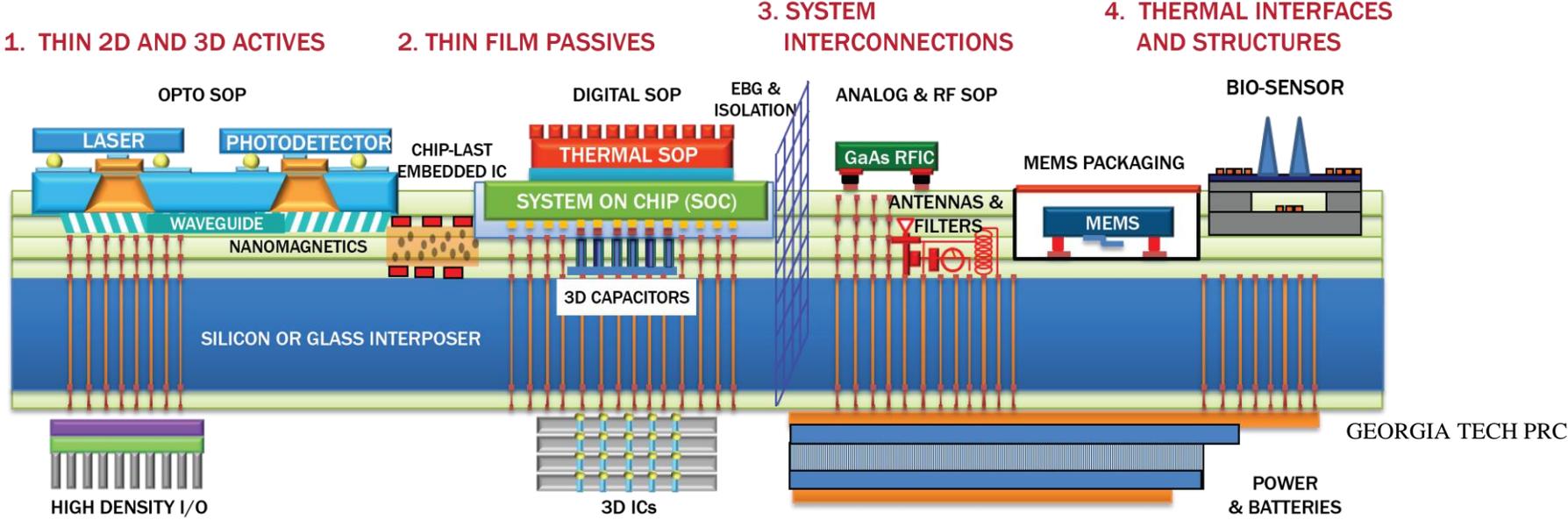
# AP Services: Embedded 2.5/3D — Wafer Reconstitution



Wafer reconstruction and adaptive substrates provide additional flexibility and next level packaging alternatives.

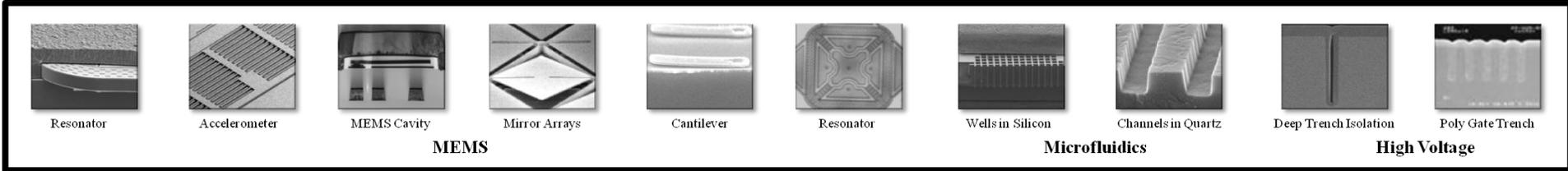


# NHanced Supports Many More Than Moore Technologies



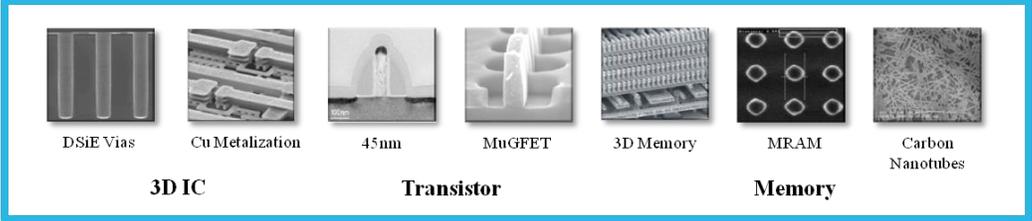
GEORGIA TECH PRC

- 5. MULTI-FUNCTION MATERIALS
- 6. MIXED SIGNAL DESIGN AND TEST
- 7. MECHANICAL DESIGN AND RELIABILITY
- 8. POWER SOURCES



Resonator
Accelerometer
MEMS Cavity
Mirror Arrays
Cantilever
Resonator
Wells in Silicon
Channels in Quartz
Deep Trench Isolation
Poly Gate Trench

**MEMS**
**Microfluidics**
**High Voltage**

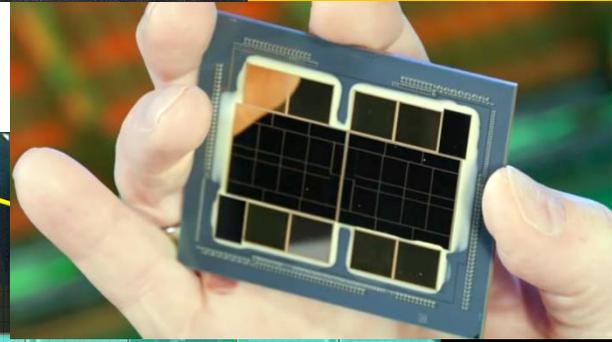
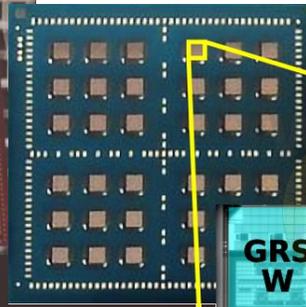
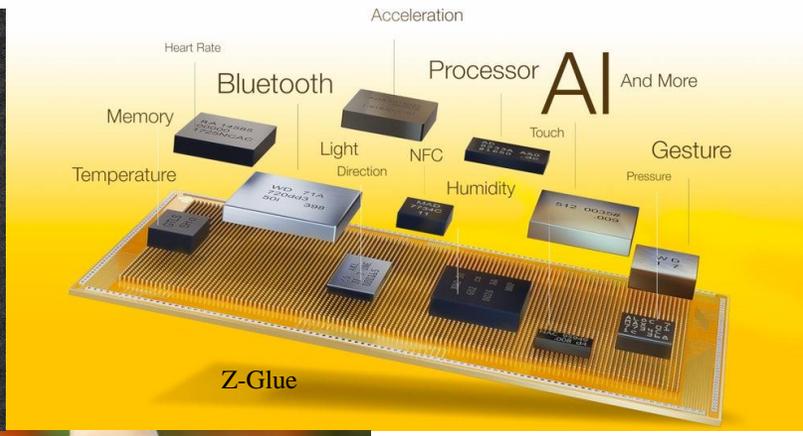
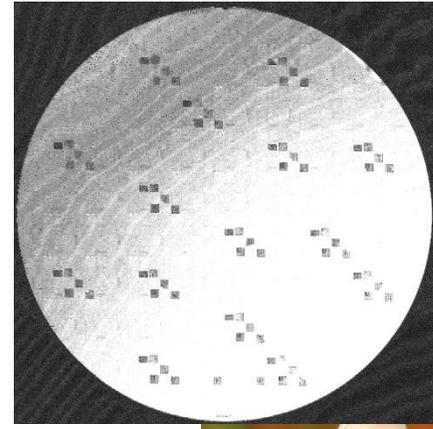


DSiE Vias
Cu Metalization
45nm
MuGFET
3D Memory
MRAM
Carbon Nanotubes

**3D IC**
**Transistor**
**Memory**

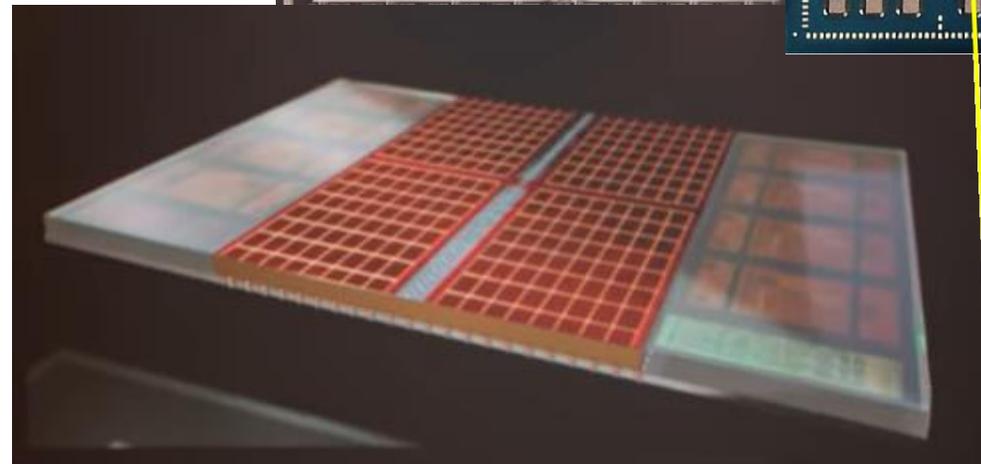
# AP Services: Chiplets

- Provides:
  - Best of Class Everything
  - Easy retargeting
  - Lower risk
  - IP reuse
  - Lower cost



Intel

AMD



GRS W	GRS N	GPIO	GRS N	GRS E
GB	PE	PE	PE	PE
RISC-V	PE	PE	PE	PE
	PE	PE	PE	PE
	PE	PE	PE	PE
GRS W	GRS S	JTAG	GRS S	GRS E

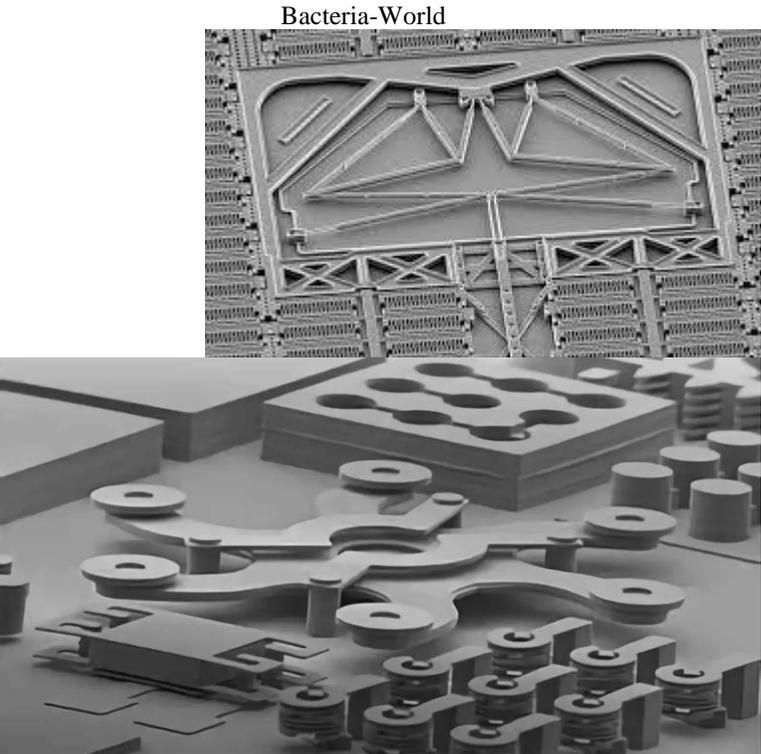


Intel

nVidia

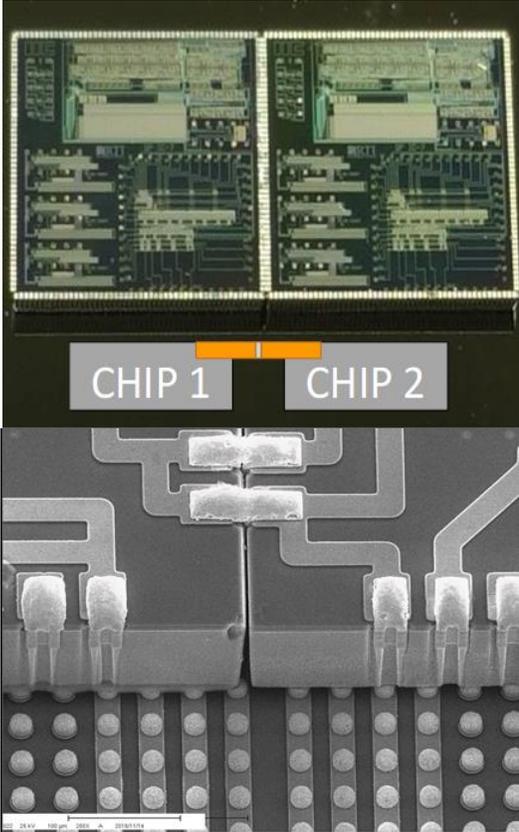
# AP Services: Micro-Connections and 3D Structures

## MEMS + Precision Electronics



techunwrapped.com

IIC



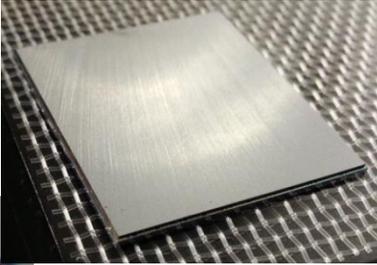
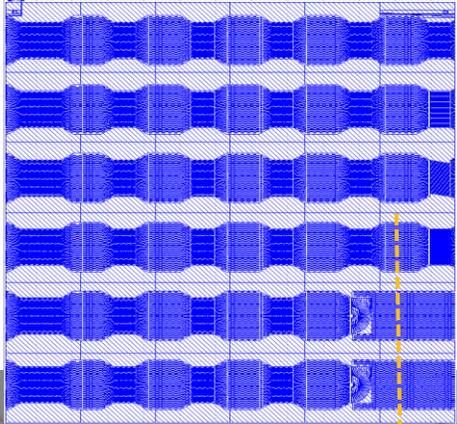
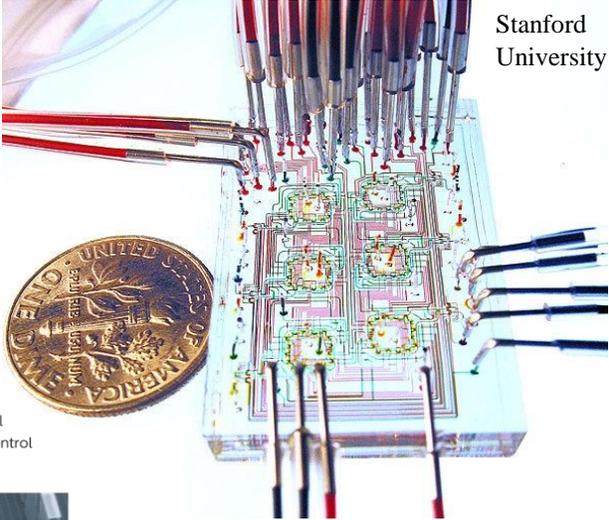
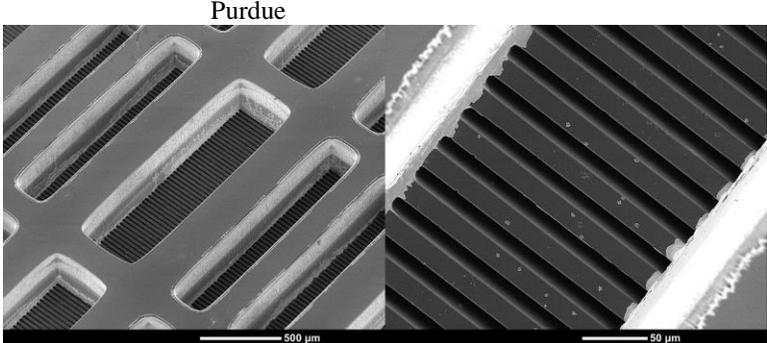
Quilt Packaging concept cross-section illustration & image of a post-reflowed QP CMOS quilt

SEM image of quilted chip-to-chip seam of >10 micron width

# AP Services: Microfluidics and Cooling

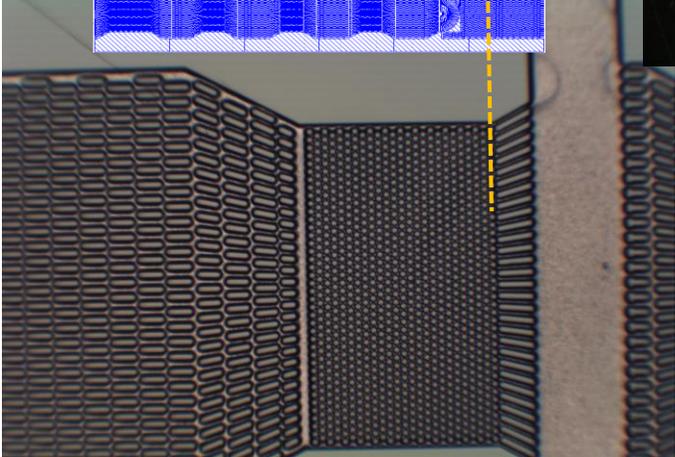
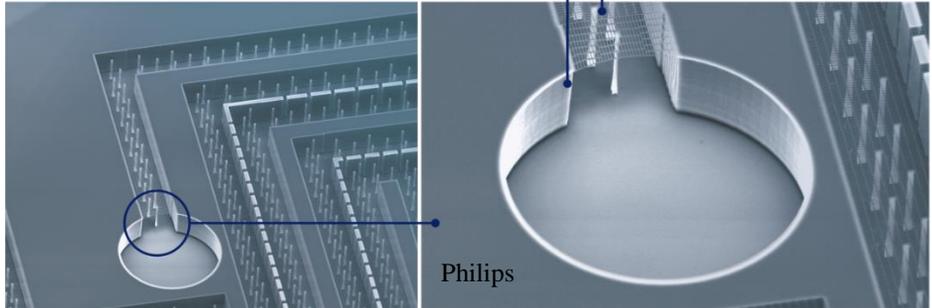
## Chip Scale Cooling For Ultra-Dense Electronics

### Biology + Electronics



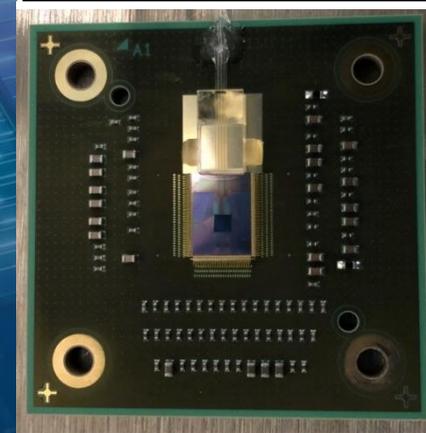
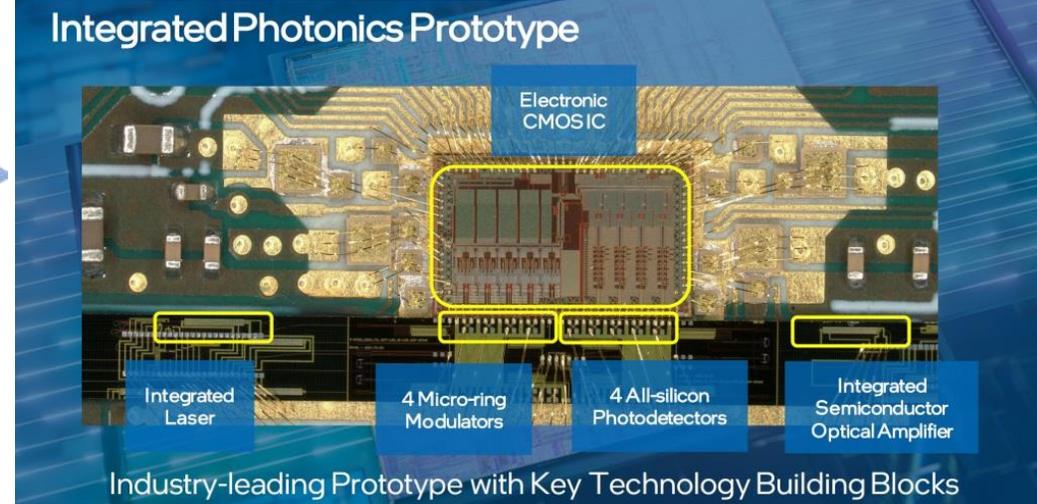
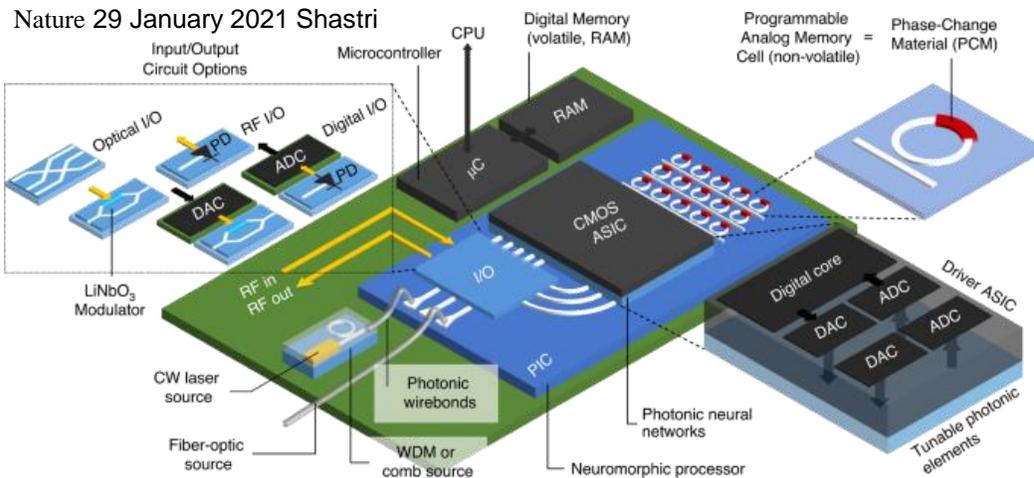
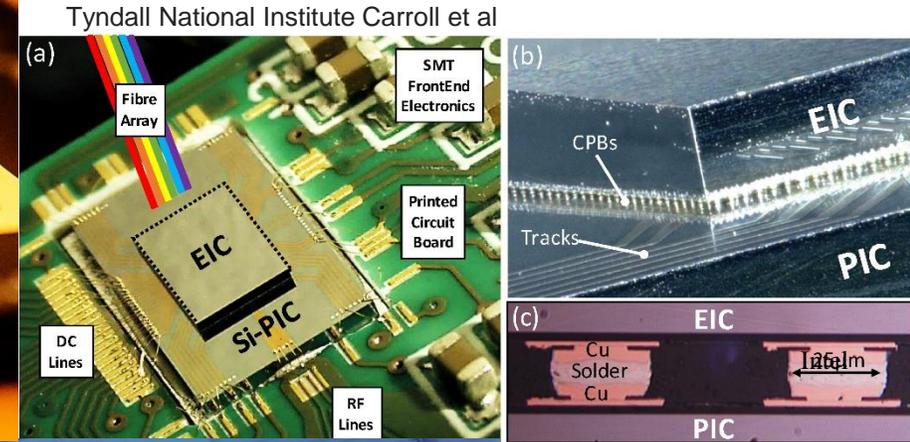
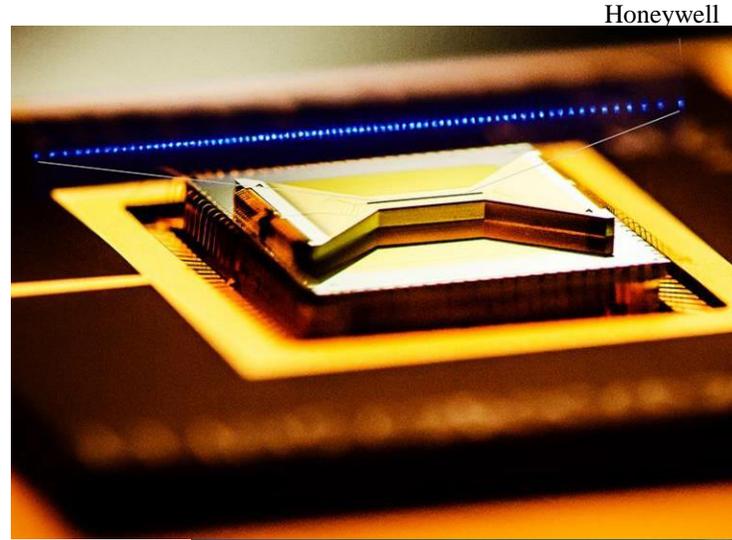
Our state-of-the-art tool set enables us to create microfluidic structures with accurate control:

- <5 degree slope control
- Sub-μm feature size control
- μm range feature size



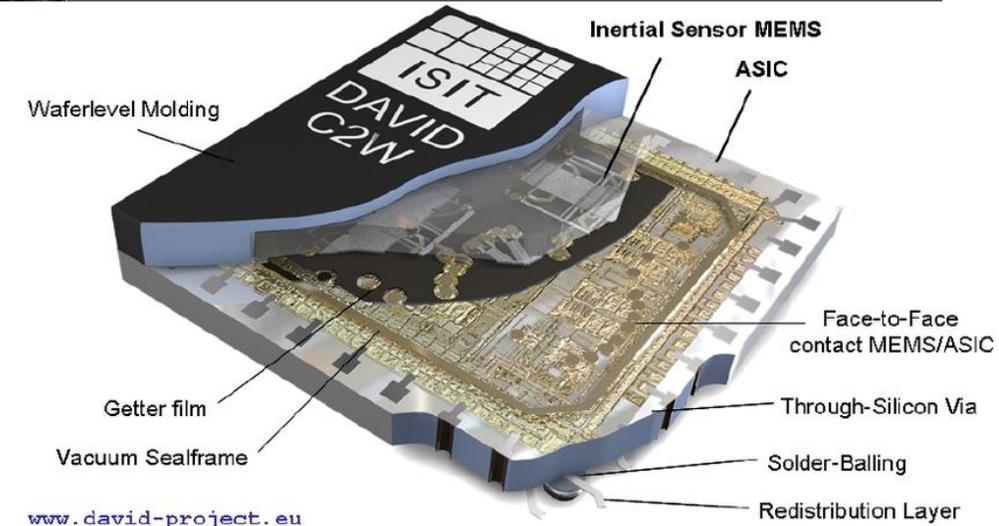
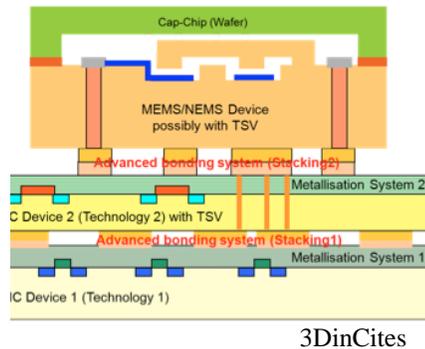
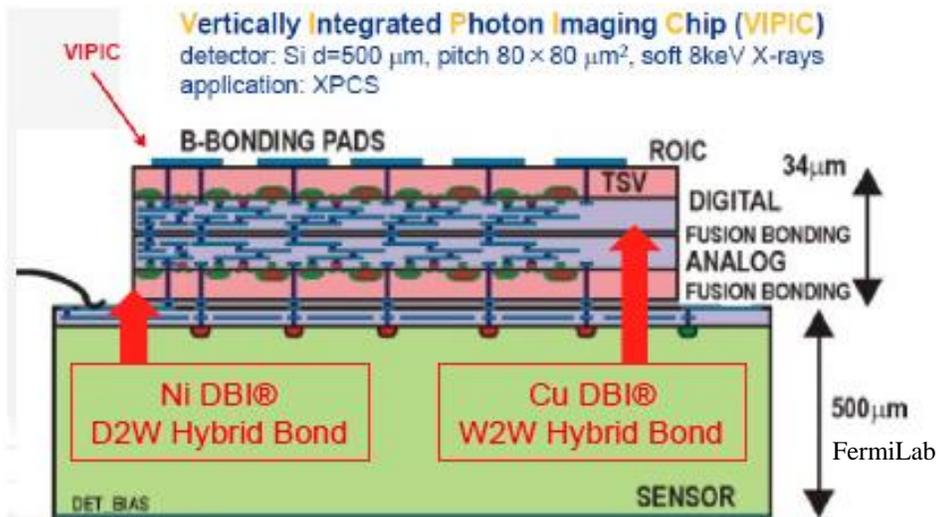
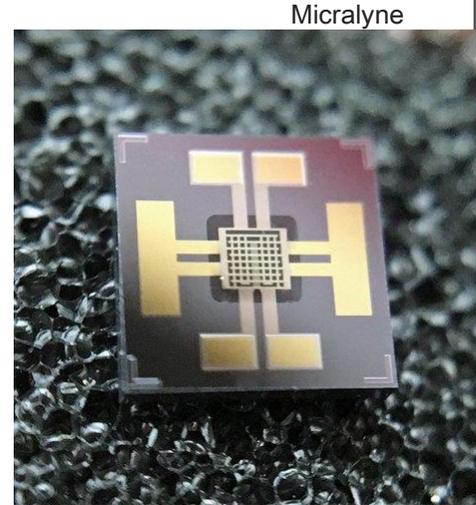
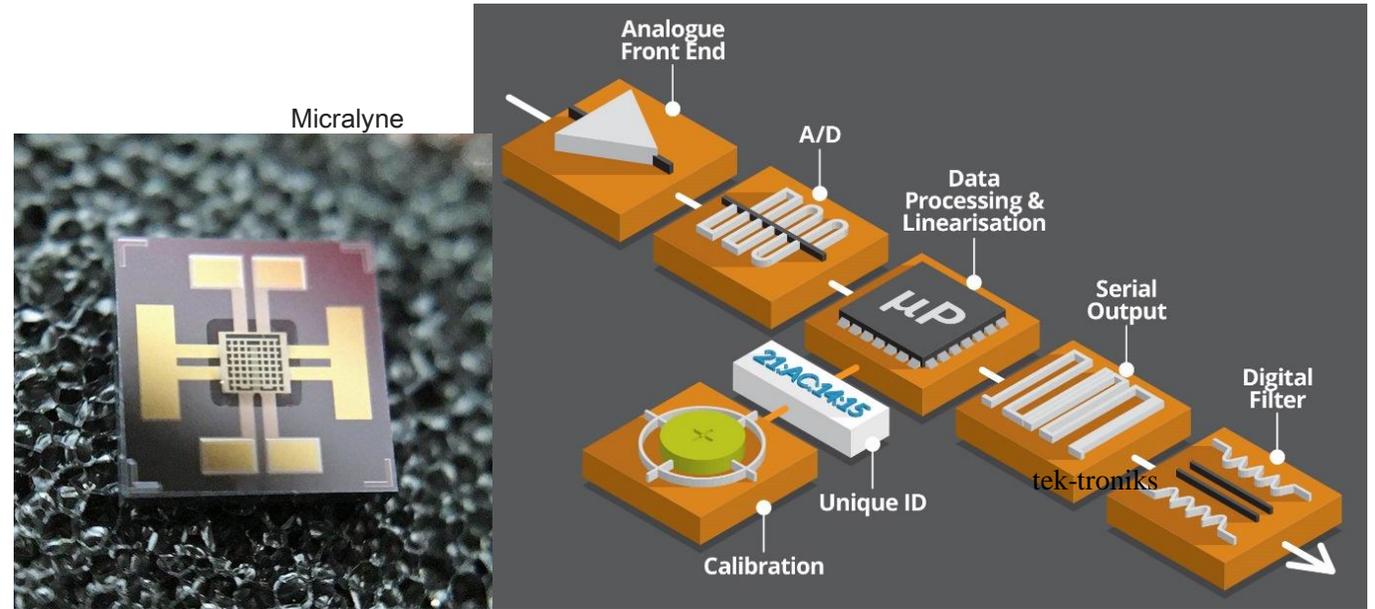
# AP Market Drivers: Photonics & Quantum

- I/O
  - Tb/s,  $\ll 100\text{fJ/b}$ 
    - SiP 500ff I/O Load
    - 2.5D 25ff I/O Load
    - 3D 3ff I/O Load
- Processing
  - “Quantum Leaps”



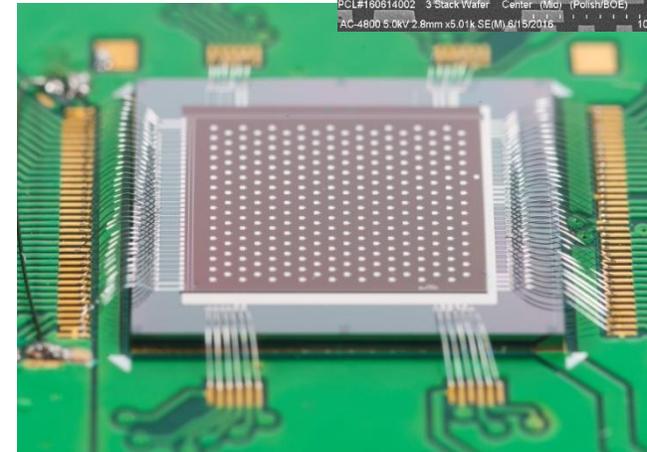
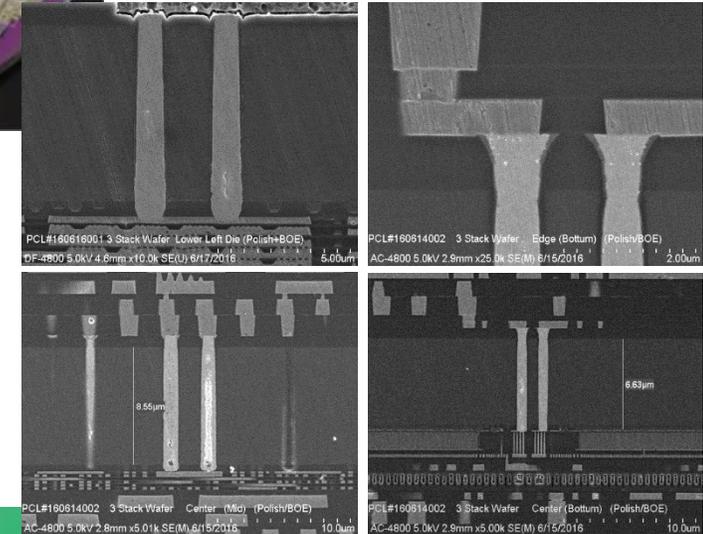
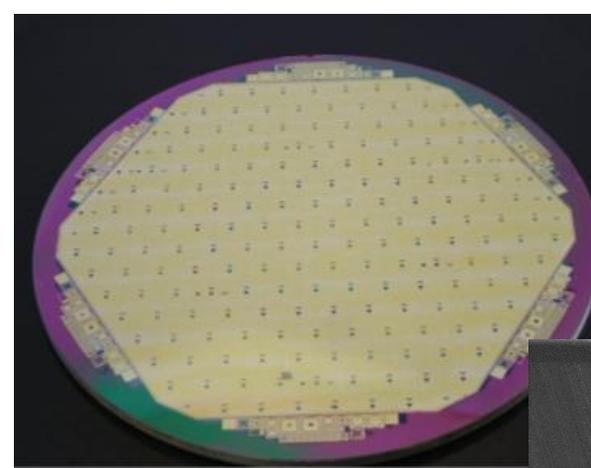
# AP Market Drivers: Intelligent Sensors and Edge Compute

- Communication is limited
  - Data movement costs power
  - Data movement costs time
  - Data movement costs money
  - You can't always "phone-home"



# NHanced Small/Medium Scale – High Touch Manufacturing

- 2.5/3D Advanced Packaging
- Si Sensors
- Commercial Development
- Mil-Aero Development and Manufacturing
  - Full BEoL
    - Niche BEoL Processes
    - Cu, Ni, Al, +
  - Split-Fab
  - High k-caps
  - ReRAM
  - 3/5 and LiNbO3 integration
  - Thick Wafer & Thin Wafer Processing
- ISO 9001
- CRADA in place for Trust
- Target market is customers needing 1 to 5000 wafers per year



# NHanced Standard Capabilities

## Advanced Packaging:

- HDI edge packaging
- Chiplet integration
- TSV insertion
- Covalent oxide bonding
- Hybrid copper and nickel bonding
  - True heterogeneous integration
- Transfer printing assembly
- Wafer reconstitution
- Die-to-die, die-to-wafer, and wafer-to-wafer 2.5D and 3D integration

## Specialized Materials:

- Interposers: silicon, glass, and fused silica
  - Optical and electrical interconnect
- Advanced substrates: silicon, GaN, GaAs, InP, GaSb, LiNbO<sub>3</sub>, BTO, SiC, etc.

## AP Assembly:

- Flip-chip
- Solder ball drop
- Co-packaged optics
- Interposer and substrate

