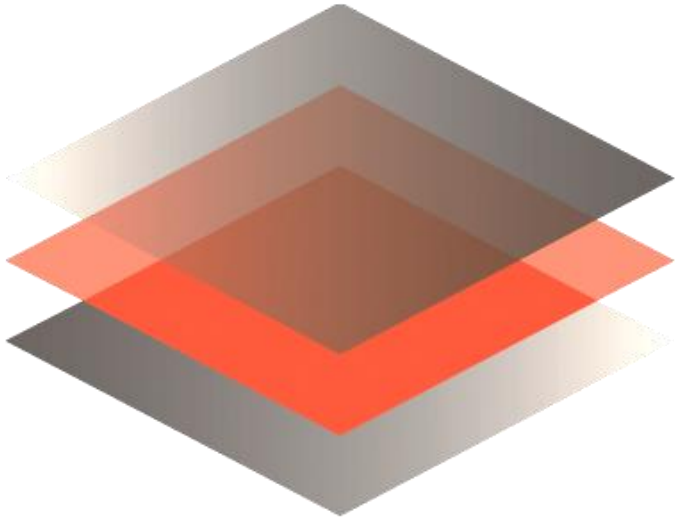
The Future Path to Heterogeneous Integration



Charles Woychik, Ph.D.
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cwoychik@nhanced-semi.com

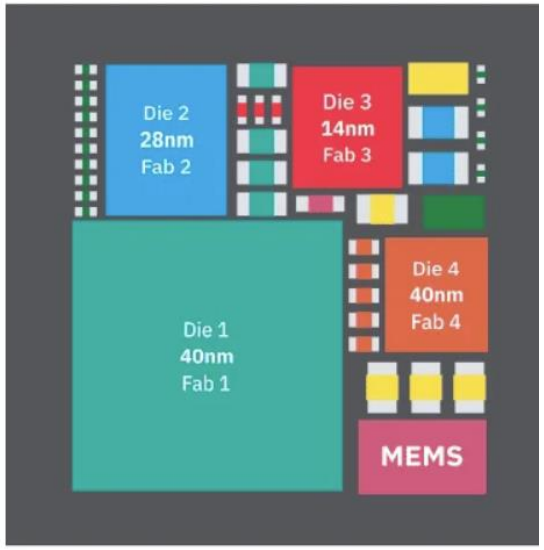
NHanced SEMICONDUCTORS

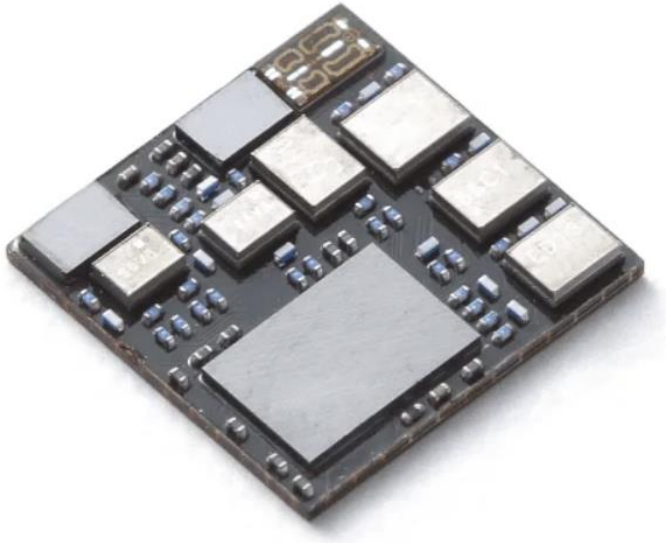
Outline

- Heterogeneous Integration – What is it?
- What is the Proper Metric?
- Markets
- What are the Core AP/HI Technologies?
- Maintaining Leadership
- Summary

ASE's Definition of HI

- **What is Heterogeneous Integration (HI)?**
- Heterogeneous Integration refers to the integration of separately manufactured components into a higher level System-in-Package (SiP) that, in the aggregate, provides enhanced functionality and improved operating characteristics. Source: Heterogeneous Integration Roadmap 2019 Edition CHAPTER 1 OVERVIEW.

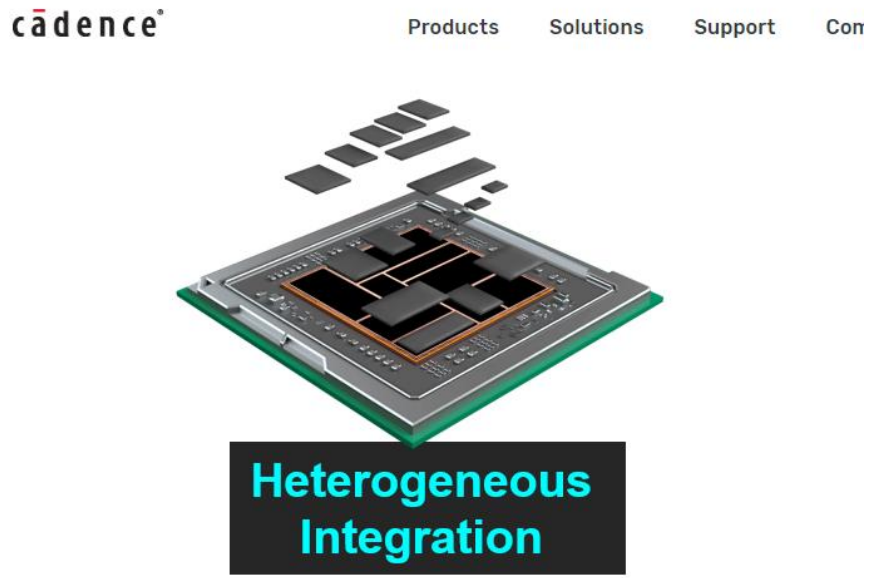




Cadence's Definition of HI

Heterogeneous Integration (HI) vs. System on Chip (SoC) – What's the Difference?

- Heterogeneous integration (HI) and SoC (system on chip) are two ways to design and build silicon chips. Heterogeneous integration aims to counter the growing expense and complexity of SoC design by taking a modular approach using advanced packaging technology.



Future Needs

- Disaggregating their chips, whether it was for yield, cost or form factor.
- Break up the large die into chiplets.
- Integration of these chiplets across different technologies is what is referred to as Heterogeneous Integration (HI).
- HI is the superset.
- HI is a term that has come into broader use in contemporary times as we take more functionality and move it upstream into the fab.
- Chiplet is designed and optimized to be integrated into a package.
- Integration of chiplets is HI whether 2.5D or 3D.

Heterogeneous Integration Finding Its Footing

162 Shares | 23 | 7 | 125

Definitions, applications, and tools are still evolving, but success stories are becoming more common.

OCTOBER 19TH, 2023 - BY: **ED SPERLING**

Semiconductor Engineering sat down to discuss heterogeneous integration with Dick Otte, president and CEO of Promex Industries; Mike Kelly, vice president of chiplets/FCBGA integration at Amkor Technology; Shekhar Kapoor, senior director of product management at Synopsys; John Park, product management group director in Cadence's Custom IC & PCB Group; and Tony Mastroianni, advanced packaging solutions director at Siemens Digital Industries Software. What follows are excerpts of that conversation. To view part two of this discussion, click here. Part three is here.

[L – R] Dick Otte, Mike Kelly, John Park, Shekhar Kapoor, and Tony Mastroianni.

HI is strictly more functions per design, because now we're exceeding the reticle limits and there is no other way to do that

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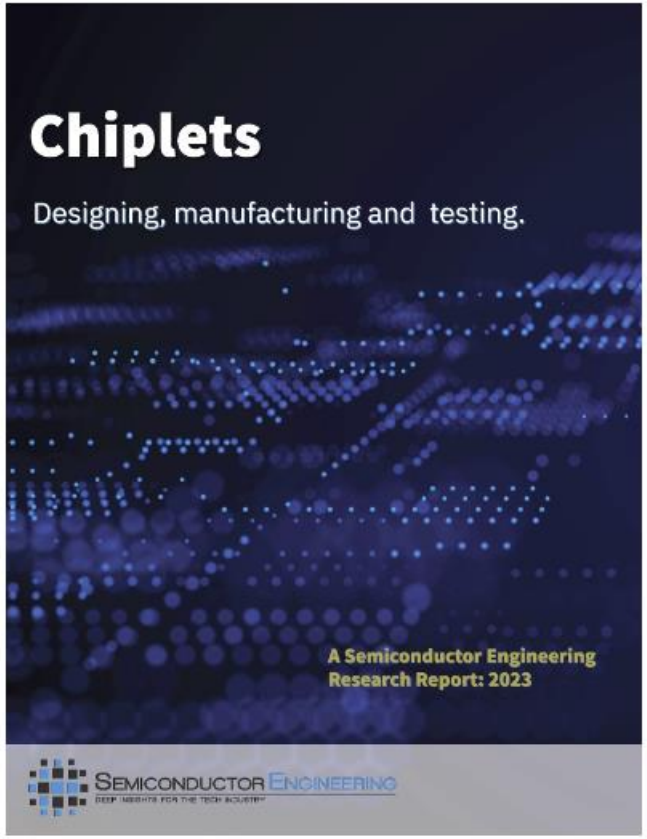
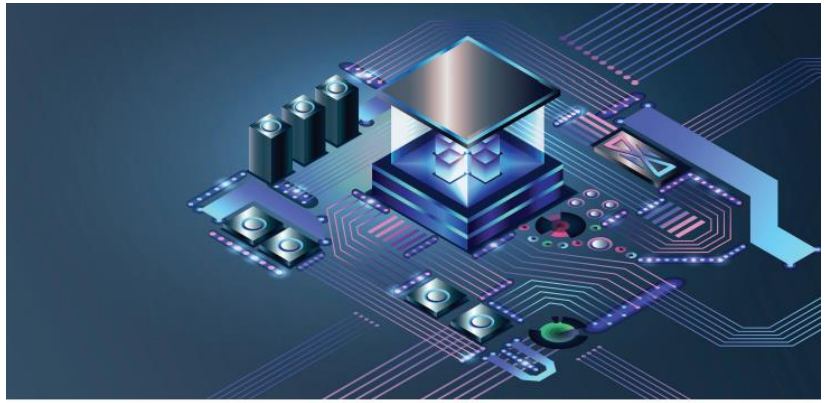
Designing, Manufacturing and Testing

- Chiplets are a disruptive technology. They change the way chips are designed, manufactured, tested, packaged, as well as the underlying business relationships and fundamentals.
- This technology creates vast new opportunities for existing chipmakers and startups to create highly customized components and systems for specific use cases and market segments.



Standardization of Chiplet Models

The Chiplet Design Exchange (CDX) proposes a set of standardized chiplet models that include thermal, physical, mechanical, IO, behavioral, power, signal and power integrity, electrical properties, and test models, as well as documentation to facilitate the integration of the chiplets into a design.



SIEMENS DIGITAL INDUSTRIES SOFTWARE

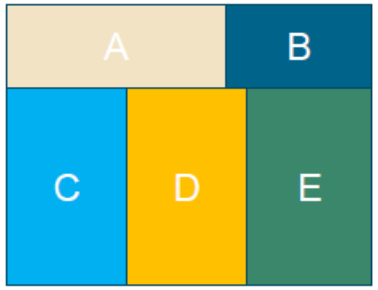
Proposed standardization of chiplet models for heterogeneous integration

Successful deployment of chiplet-based devices requires the adoption of standardized chiplet models to establish this emerging ecosystem.

Technology Drivers for Chiplets

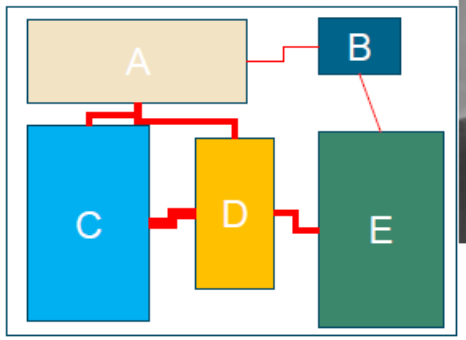
Drivers for Chiplet Integration

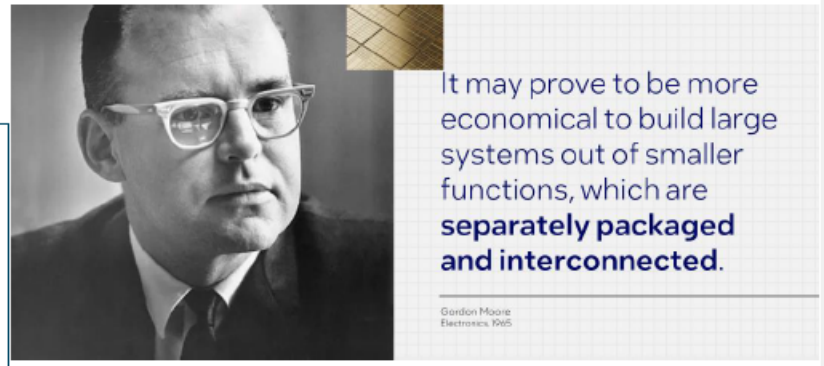
SOC



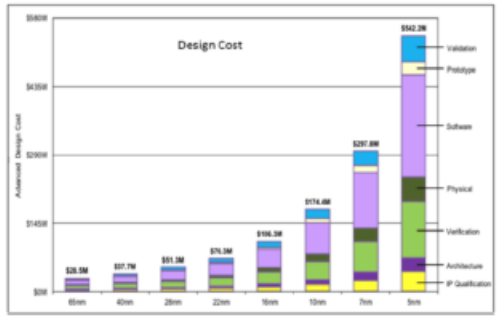
End of Cost Advantage of Moore's Law

Shared Package





- Difficult
- Very Costly
- Low Initial Die Yield



Pros

- **SWAP**
- Flexibility
- Optimized Performance
- Lower Power
- Shorten Time-to-Market
- Gordon Moore predicted that eventually one would go to packaging individual chips – Original paper.
- Thermal optimization
- Spin multiple products faster

Cons

- **Create System Integration Ecosystem (Supply Chain and Business).**
- KGD – Known Good Die
- Establish a pull by customers
- Standards
- Software Design Tools
- Yield Loss Ownership

Design cost to scale down to 5nm node.
Reference: Moore's Law is Dead – Long Live the Chiplet, Paul McWilliams 9-30-2022.

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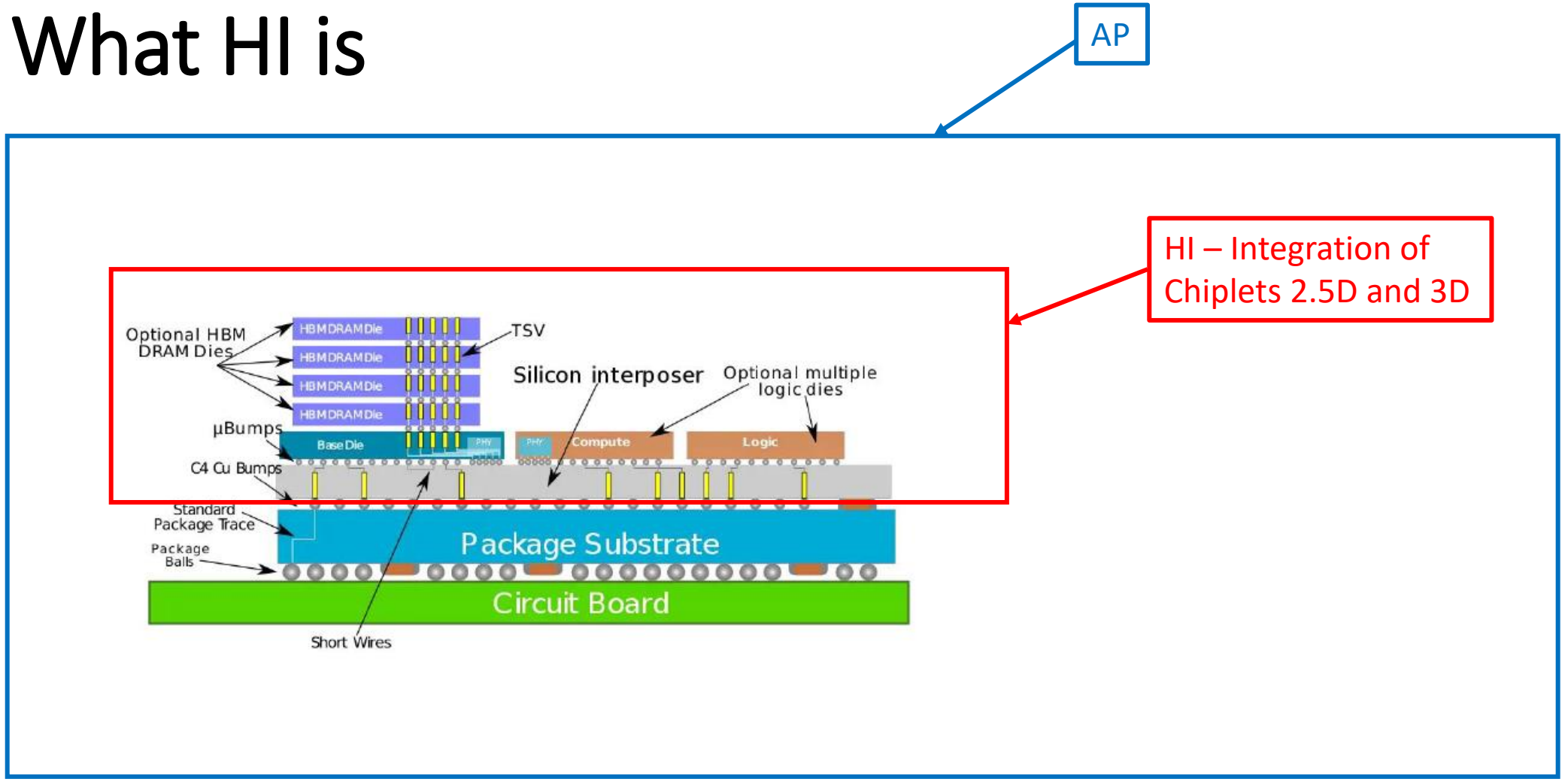
This is What HI is



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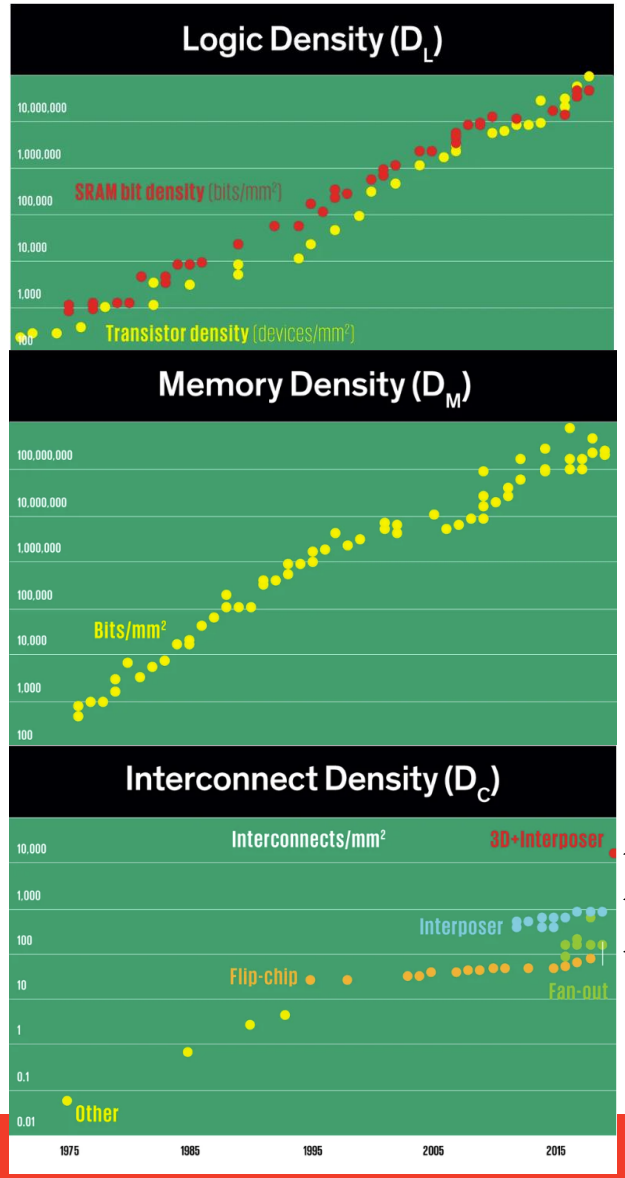
What's the Right Performance Metric?

- Moore's Law describes the shrinkage of transistors. The performance of a semiconductor technology node system is misleading because the node size has been reduced much faster than the transistor pitch and is no longer a good metric of system performance.
- The technology node picture obscures the fact that alternative methods to node shrinkage are being developed and used to drive computing performance forward.

Meeting of Minds

- Prominent group of academics got together at UC Berkley to come up with their own metric in June 2019
- Chenming Hu, Tsu-Jae King Liu and Jeffrey Boker, invented FinFET
- Prof. H. S. Philip Wong, Stanford & VP R&D TSMC
- Subhasish Mitra, codeveloper first carbon-nanotube-based computer
- James Plummer, former dean of engineering at Stanford and former board member of Intel

LMC Method



- Focus on key contributors to the overall speed and energy efficiency of a computing system
  - D_L is the density of the logic transistors
  - D_M is the density of the main memory
  - D_C is the density of the interconnects between the processor and memory (package level technology)

Reference: "A Better Way to Measure Progress in Semiconductors," Samuel K. Moore, IEEE Spectrum, 21 July, 2020

Using µbump

3D with Si-Interposer (>100X FCA)
2.5D with Si-Interposer (>10X FCA)
FCA on organic buildup

Using Hybrid Bonding

Further increases interconnect density

Gil Fountain – Adeia

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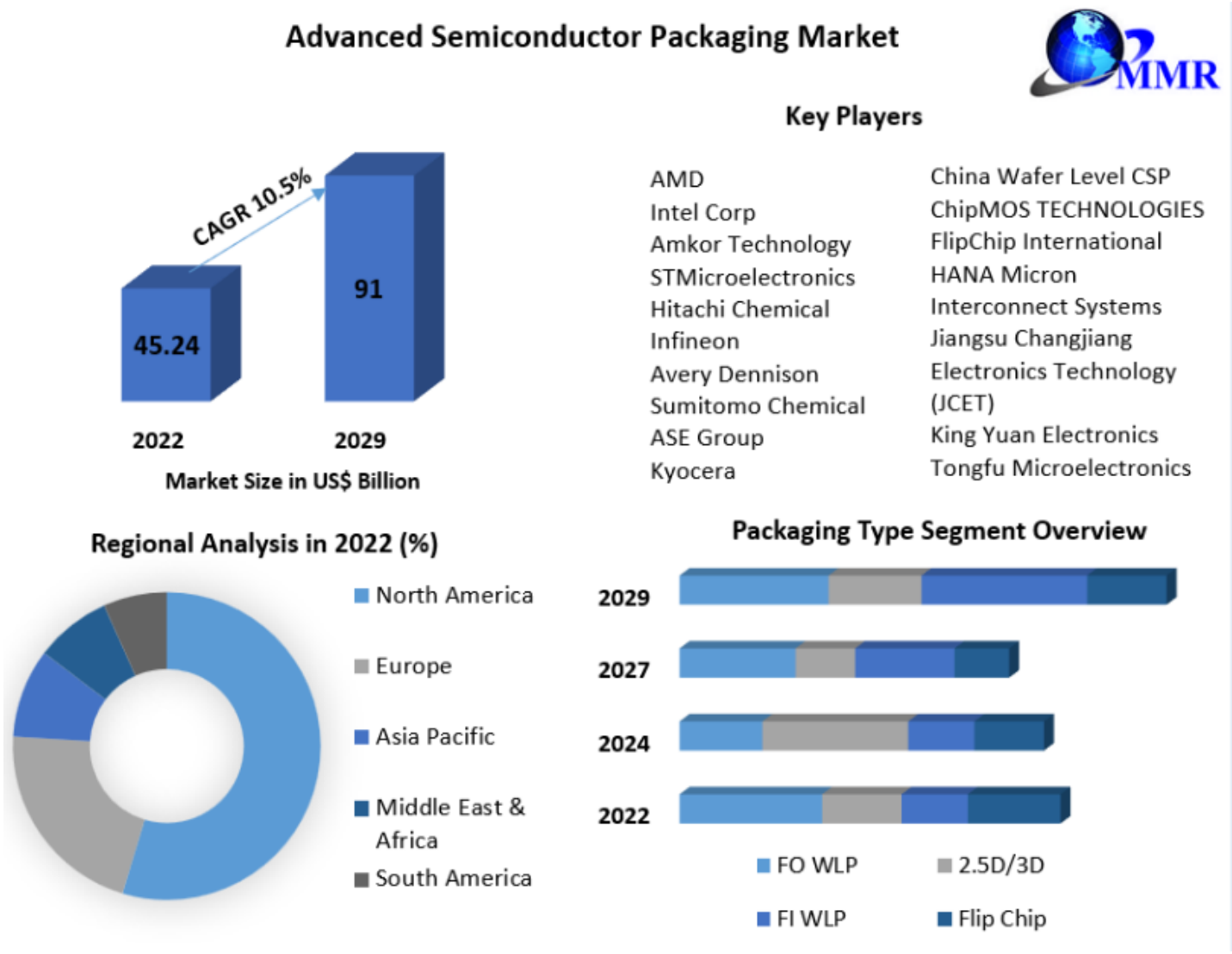
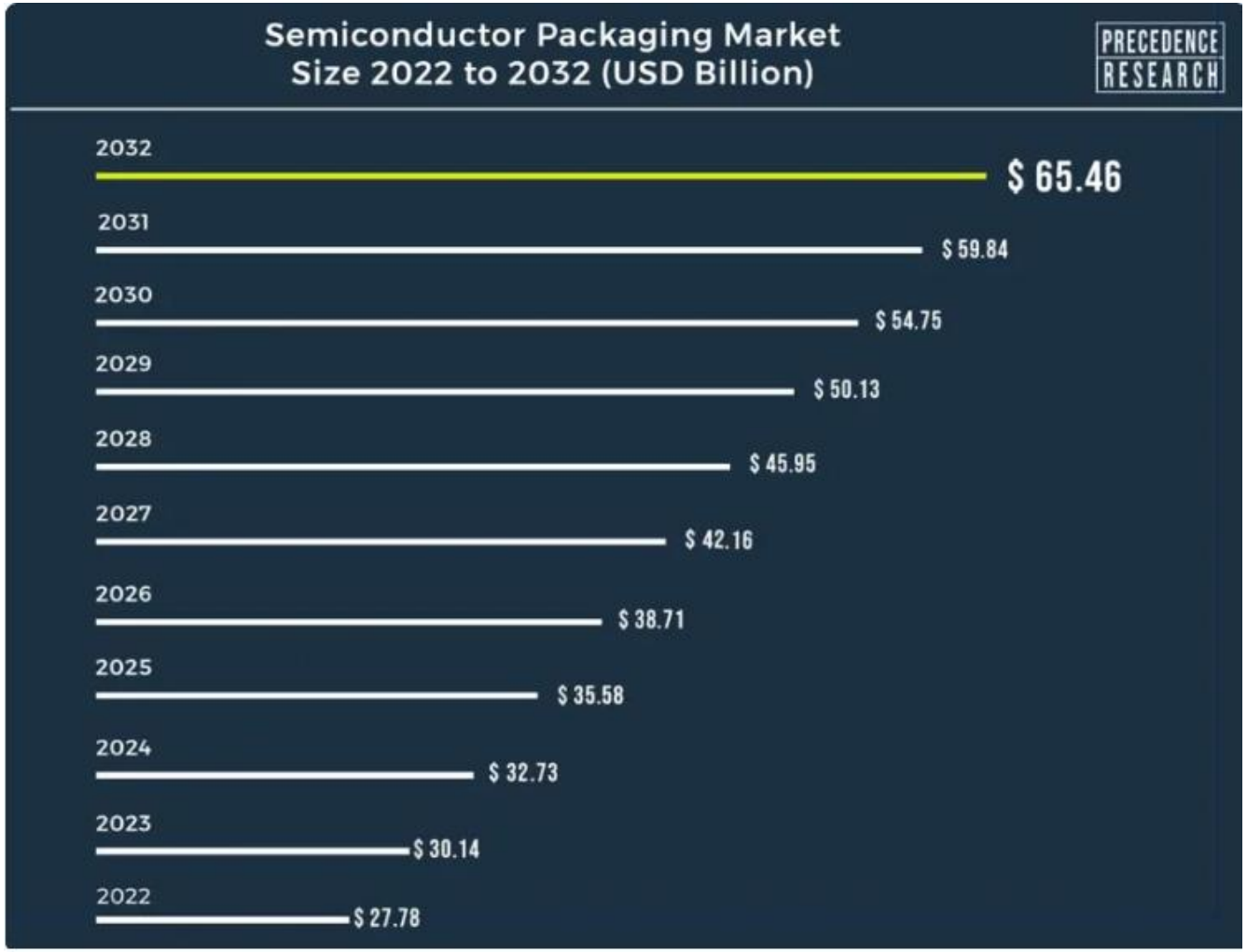
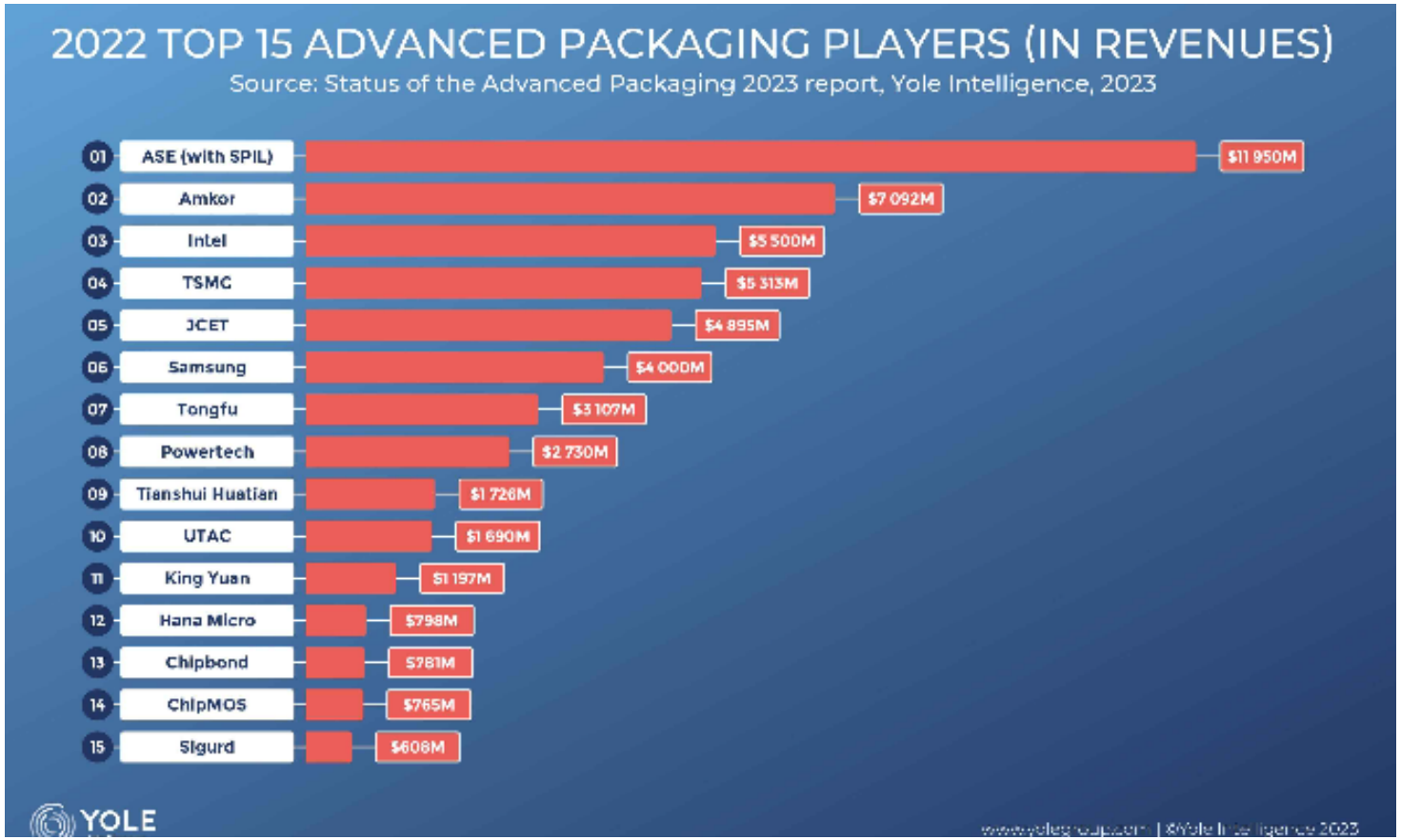
Global AP Market



Global Packaging Market



Domestic packaging industry



No North American OSAT

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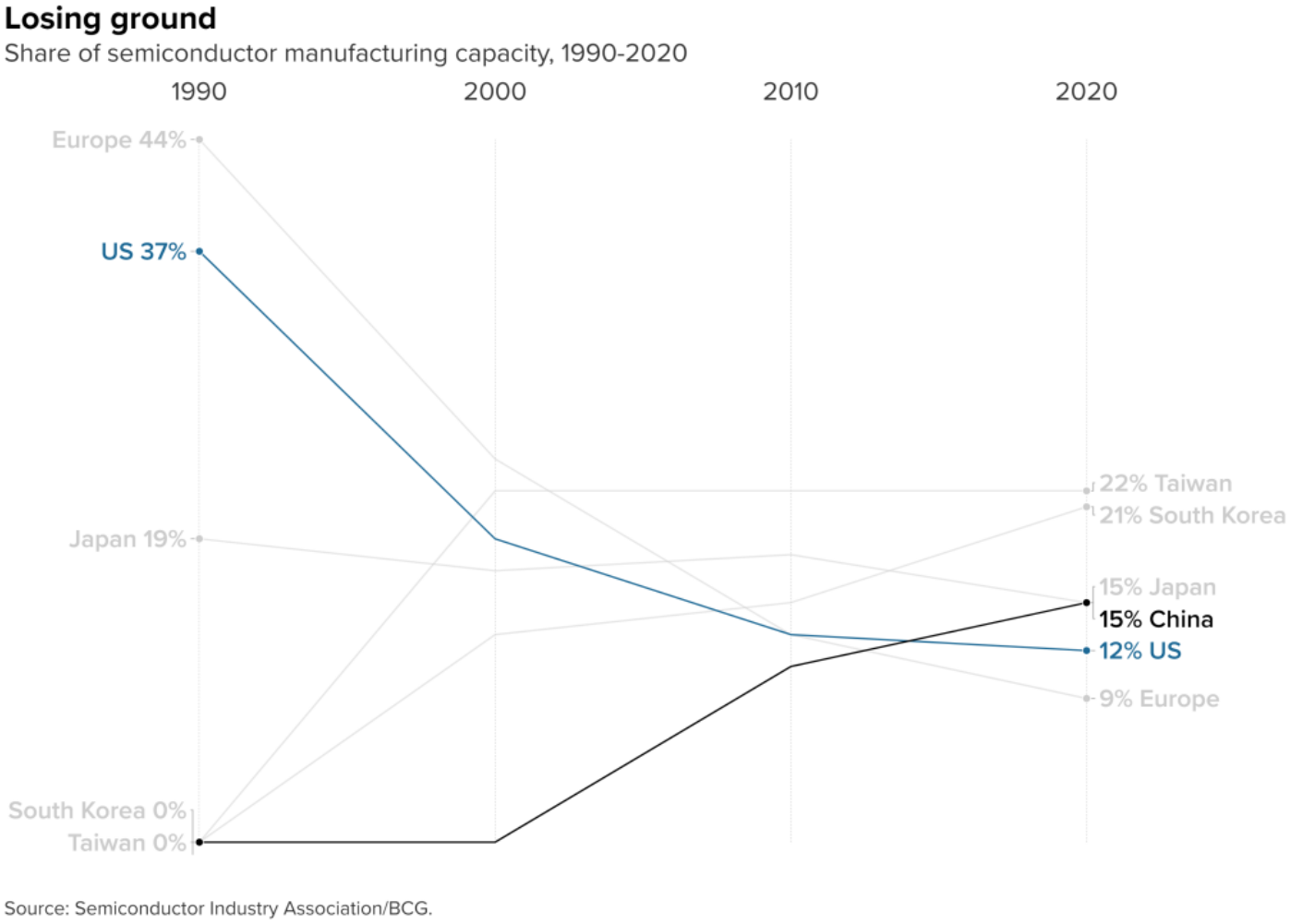
Semiconductor Mfg. Capacity



Global Landscape

North America is in a Weak Position for AP/HI

Reference: Yole 2023

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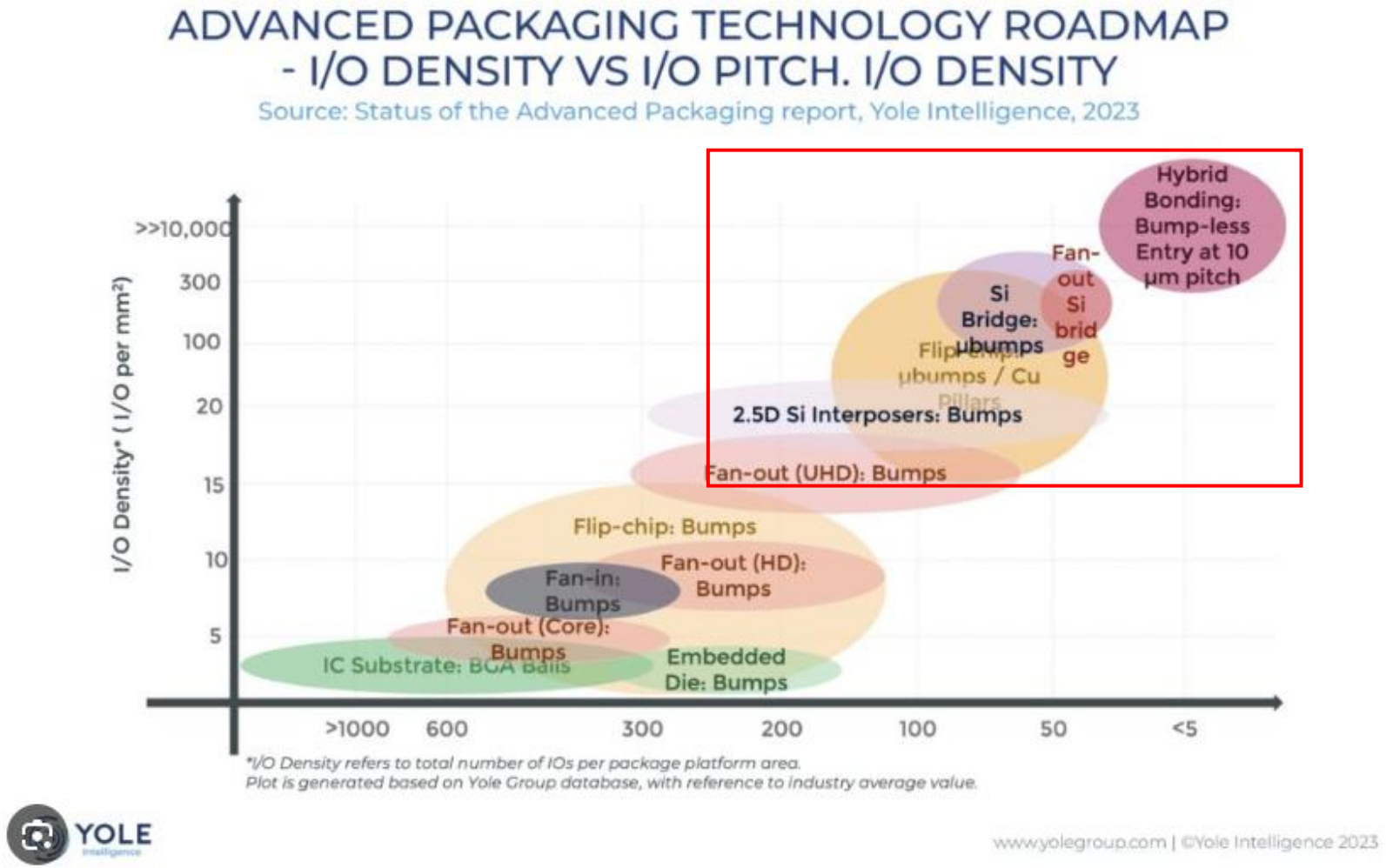
AP Roadmap



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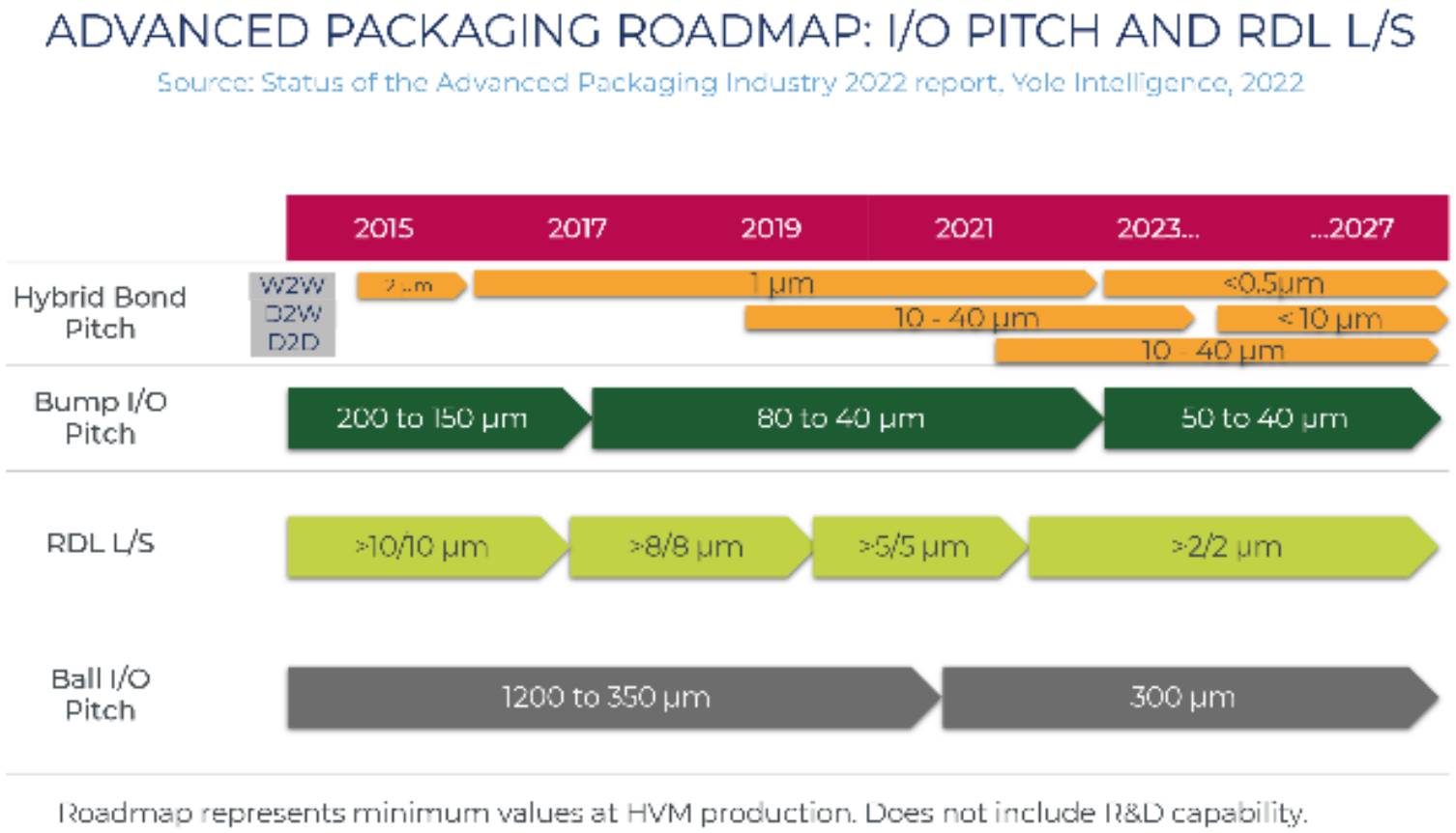
AP Roadmap



YOLE

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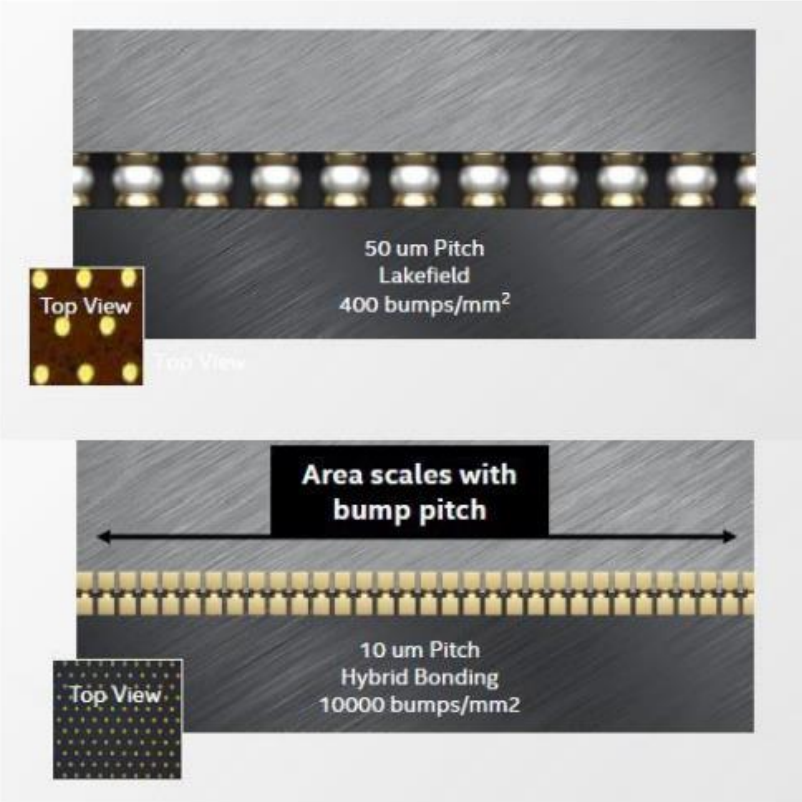
Packaging Trends

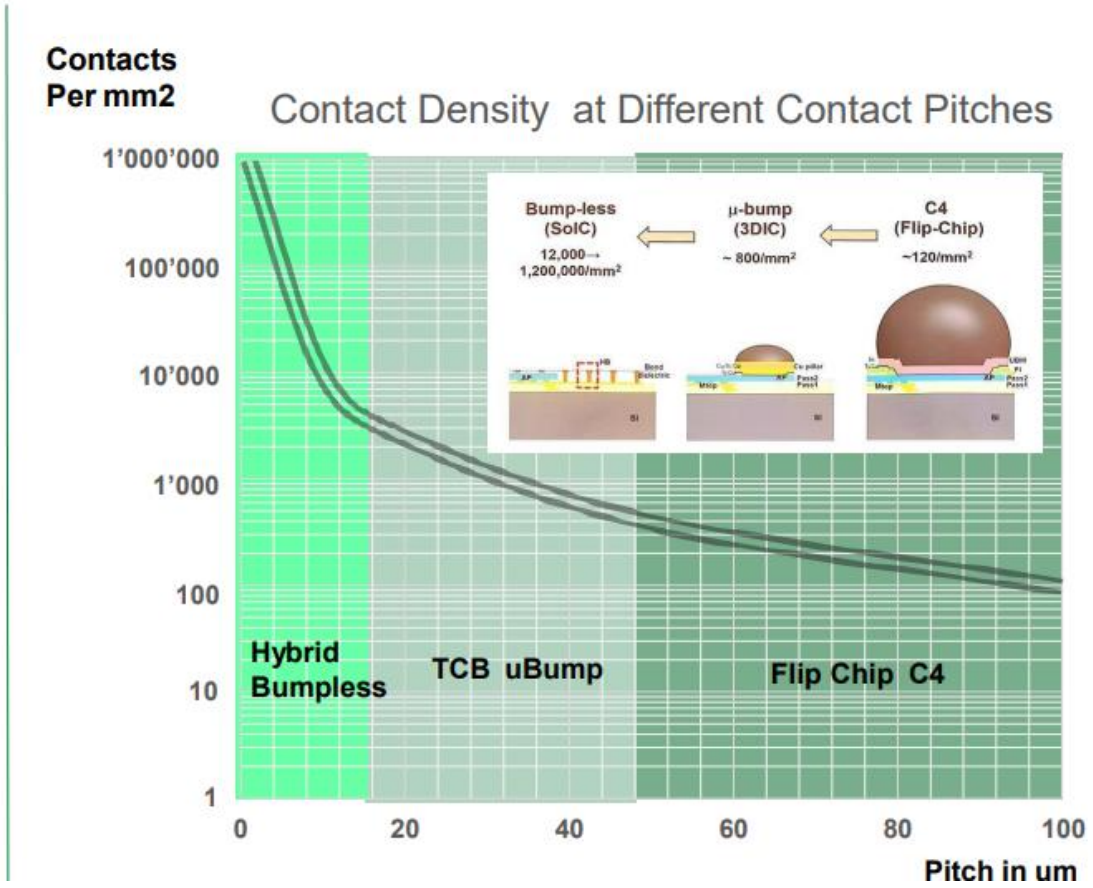
- 2.5D and 3DHI Enabling more functionality
- HI enables a near monolithic performance
- Soldering has limitations → Hybrid bonding

Reference: Intel

Hybrid Bonding is a Game Changer

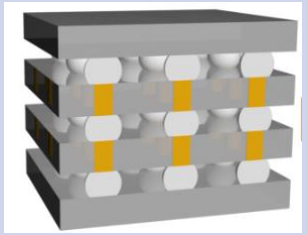
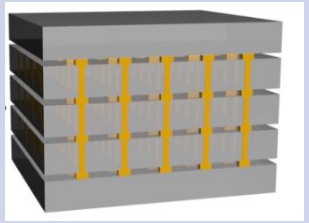
MORE DATA =>MORE CONTACTS

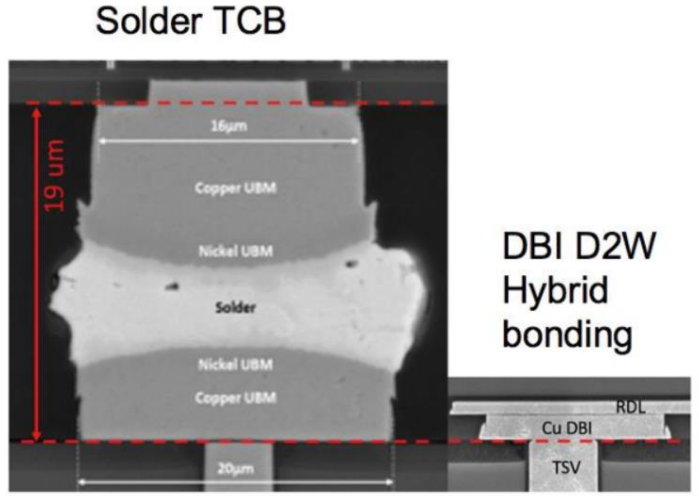




Reference: BESI

Hybrid Bonding Advantages

µ-Bump	Hybrid Bond
	
• Underfill thermal conductivity • Large temperature delta between die	• All inorganic materials • No underfill or UBM • Improved thermal & electrical performance
• Complex assembly process • Lithography, plating solder • UBM on both sides	• Reduced process steps • Lower cost
~40um pitch 625 I/O per mm^2	< 1um pitch 1.2M I/O per mm^2



Die to Wafer Hybrid Bonding: Multi-Die Stacking with Tsv Integration

Guilian Gao, J. Theil, G. Fountain, Thomas Workman, Gabe Guevara, C. Uzoh, D. Suwito, Bongsub Lee, K.M. Bang, R. Katkar, L. Mirkarimi less ·

Published in International Wafer Level... 13 October 2020 · Engineering, Materials Science ·
2020 International Wafer Level Packaging Conference (IWLPC)

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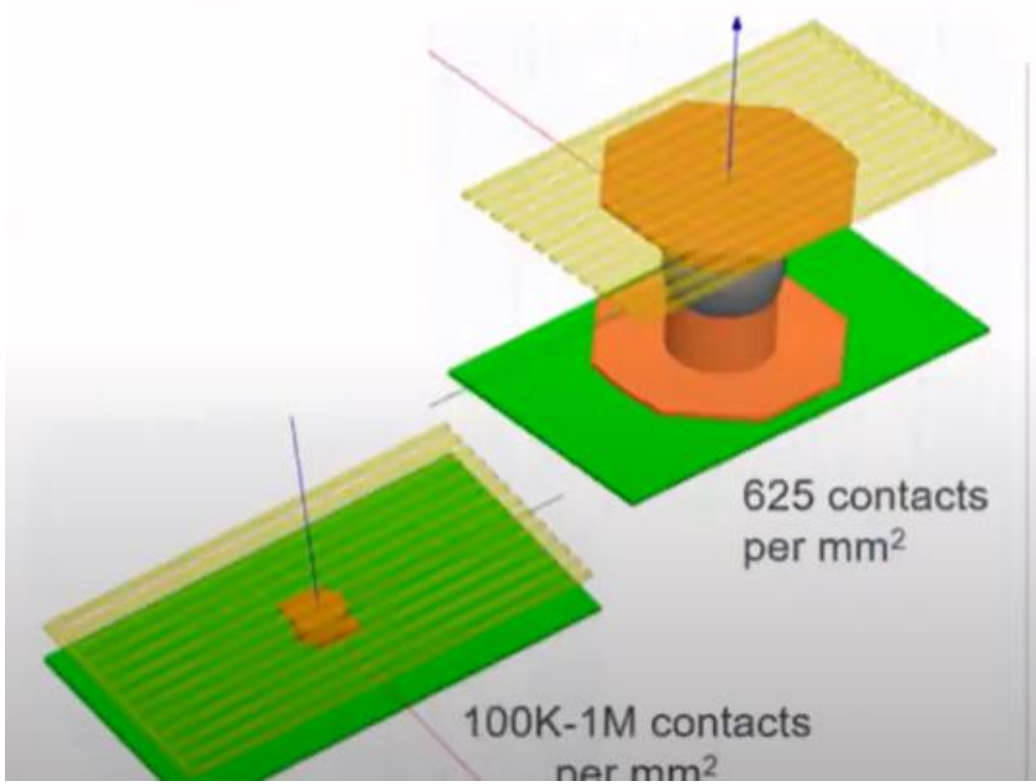
Electrical Performance Improvement with Hybrid Bonding



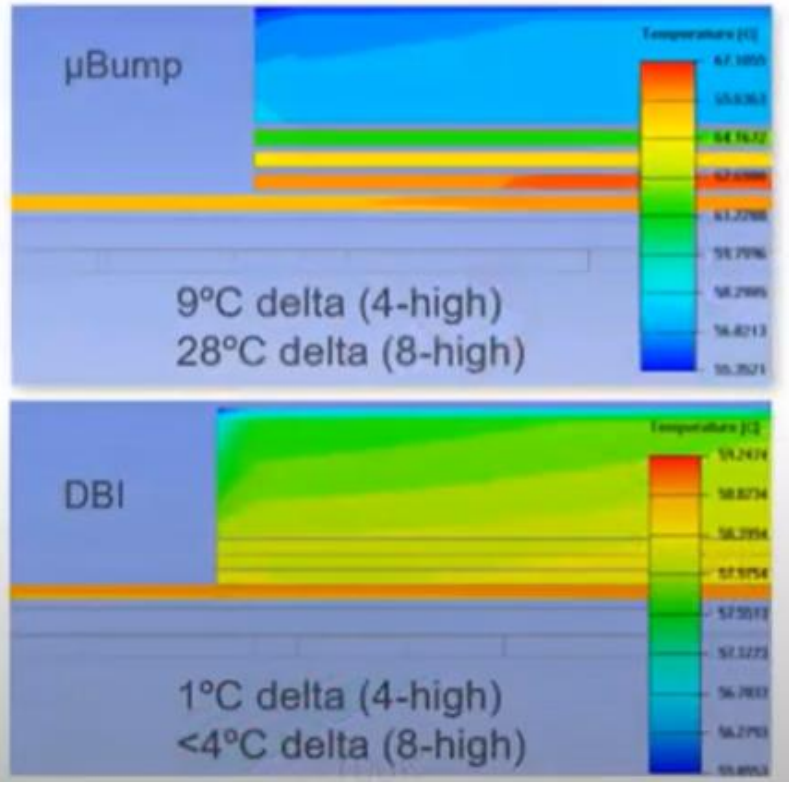
- ***Smaller electrical load means less power***
- ***1/50th size of typical µbump UBM pad***
  - 96% less Capacitance (faster)
  - 64% less Resistance (lower DC power)
  - 92% Less Self-Inductance (less signal distortion

	DBI 5 um Pad	µBump 40um pad
DC Resistance (mohm)	11.7	32.7
Self Inductance (pH)	2	25.3
Capacitance (fF)	6.1	141.7

Ref: A. Agrawal et al, ECTC 2017

Akash Agrawal et al., ECTC 2017

Thermal Performance Improvements

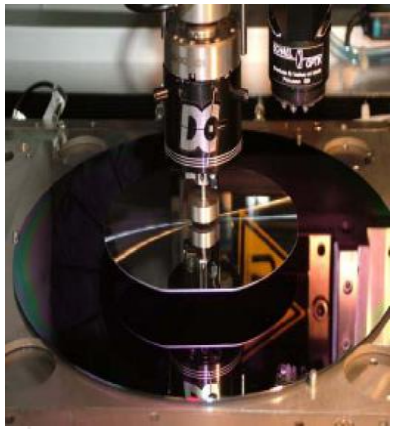


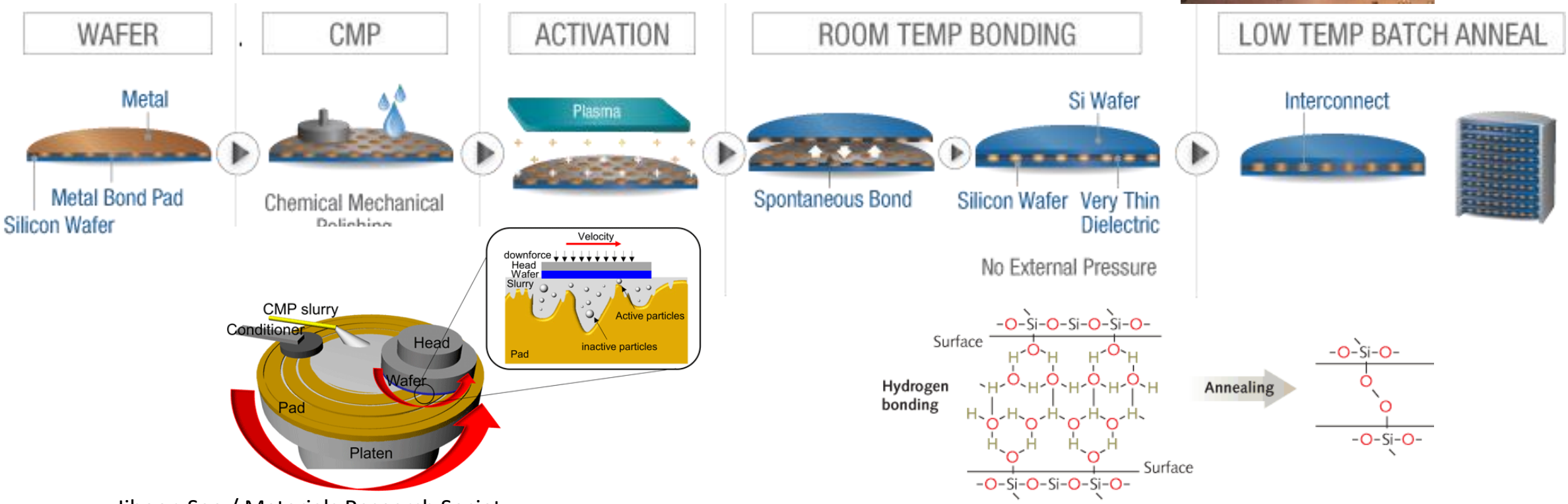
	HBM–4Die Stack		HBM–8Die Stack	
	µBump	DBI	µBump	DBI
	Forced Convection (3m/s); 25°C			
Total Power (W)	10	10	18	18
T_J (°C)	67 →	59	95 →	70
ΔT btwn die(°C)	9 →	1	28 →	4

Stack Behaves Like a Single Die

Akash Agrawal et al., ECTC 2017

DBI®: Low Temperature Hybrid Bonding Process



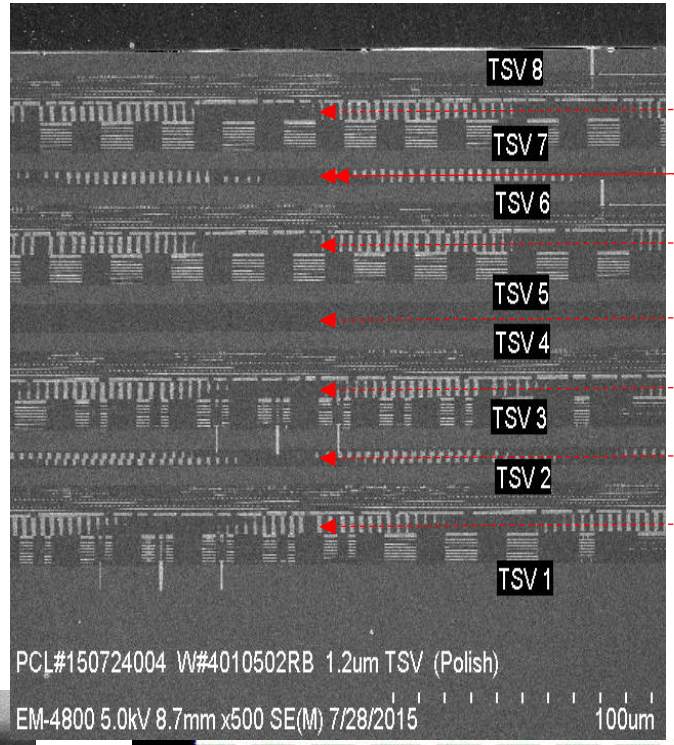


Jihoon Seo / Materials Research Society

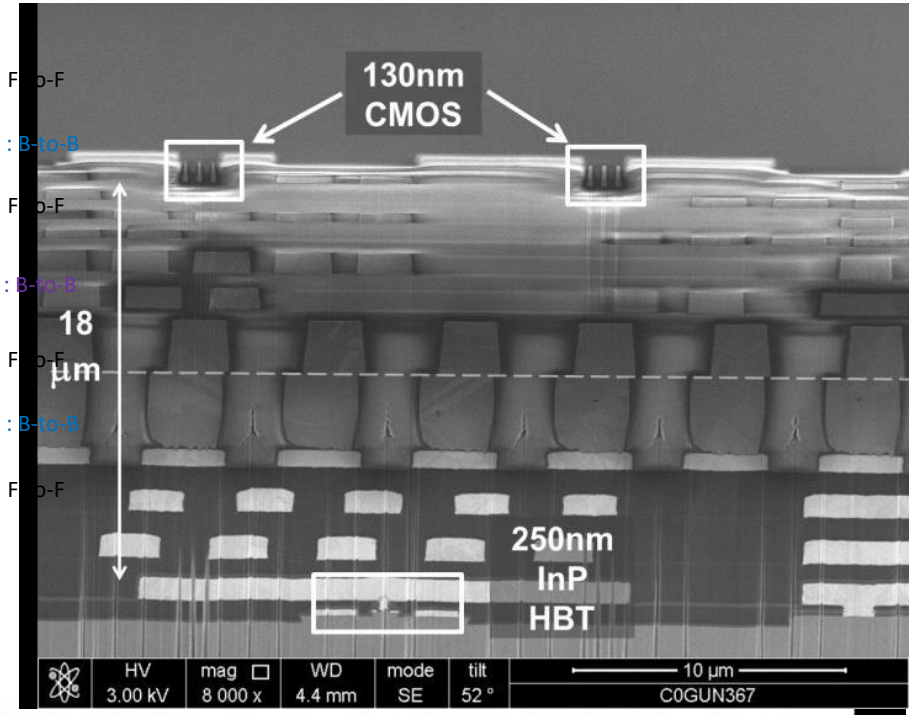
AP Bonding

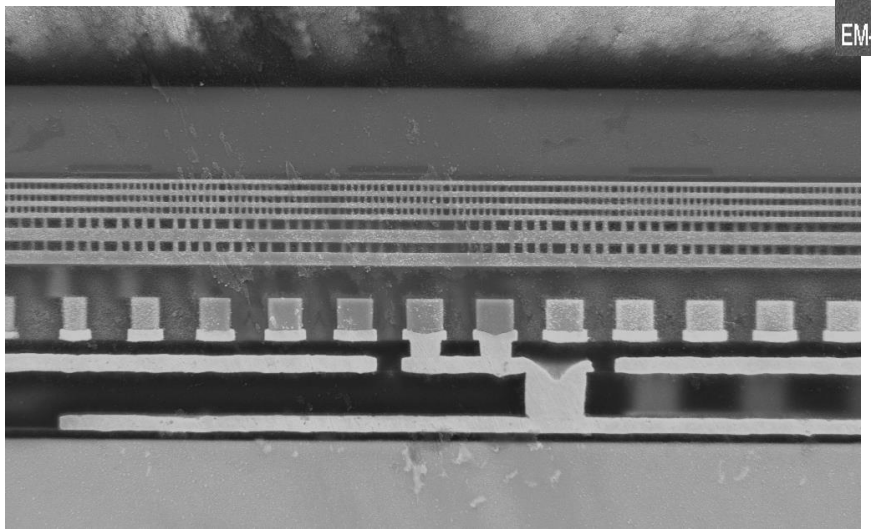
Millimeters ⇒ Microns
Kilograms ⇒ Grams

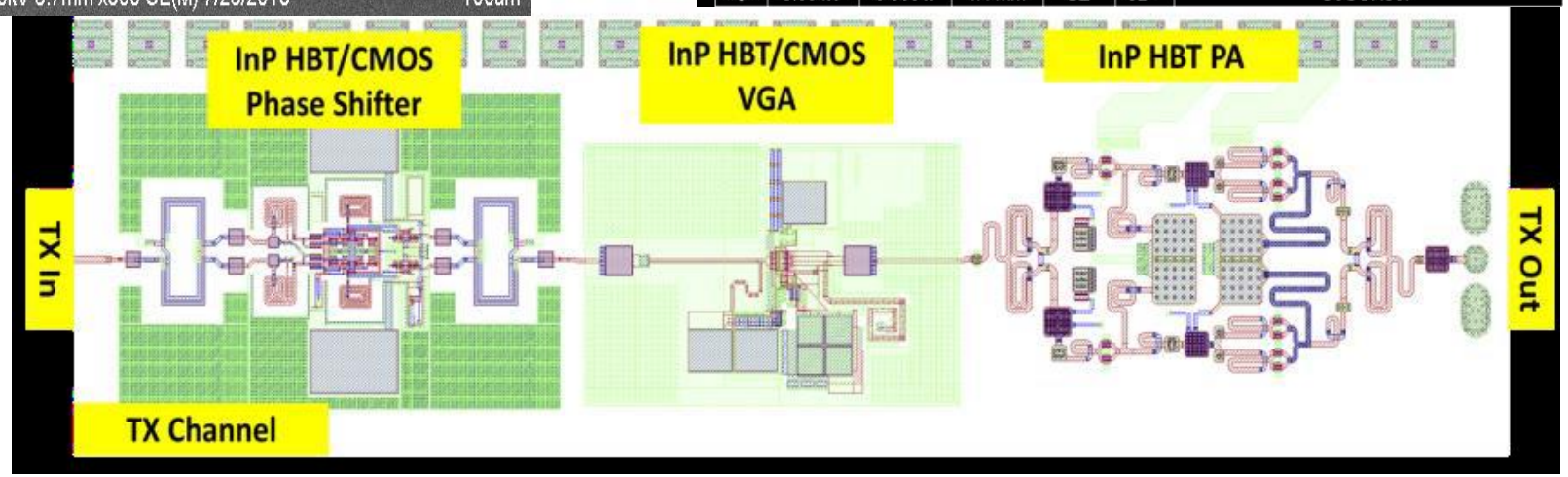
Mixed Materials
Best of Class



1st bonding: F-to-F
2nd bonding : B-to-B
1st bonding: F-to-F
3rd bonding : B-to-B
1st bonding: F-to-F
2nd bonding : B-to-B
1st bonding: F-to-F







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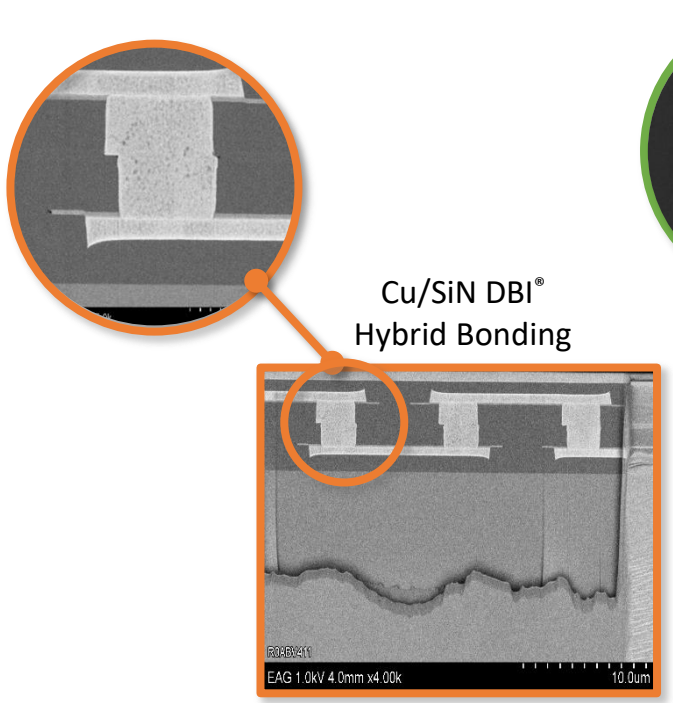
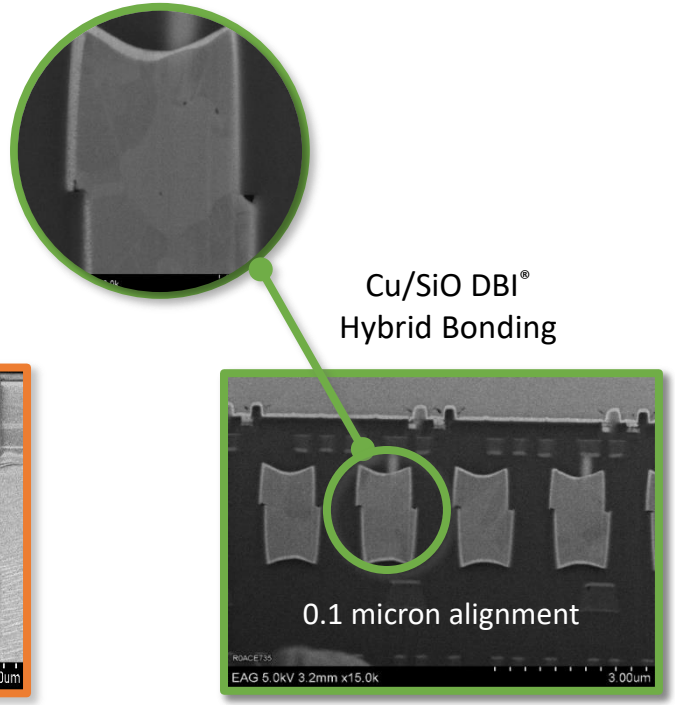
Hybrid Bonding Interconnect Pitch Scaling



Cu/SiN DBI®
Hybrid Bonding

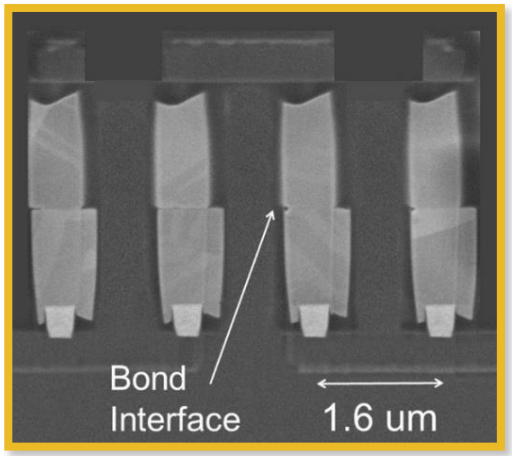
10 µm DBI® pitch, 300°C



Cu/SiO DBI®
Hybrid Bonding

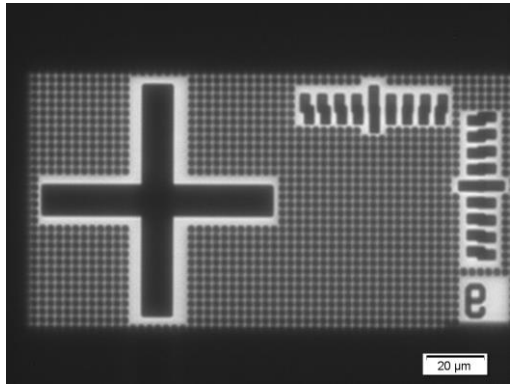
1.9 µm DBI® pitch, 300°C

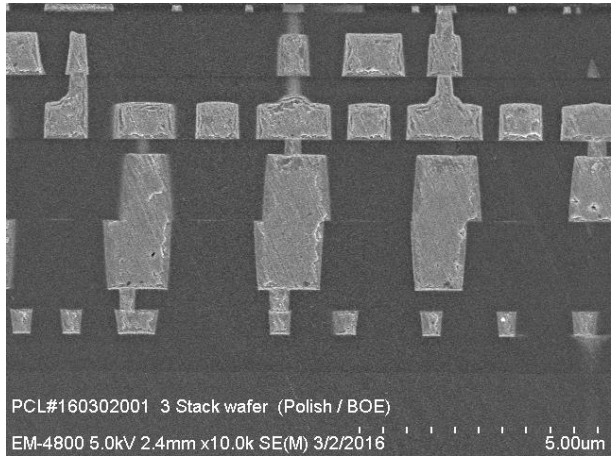
Scalable To < 1um Pitch
0.8um Pitch Demonstrated



1.6 µm DBI® pitch, 300°C

- 3sigma < +/- 1µm misalign performance
- Production Minimum pitch = 2.44µm
- Best alignment is achieved with face-to-face bonding





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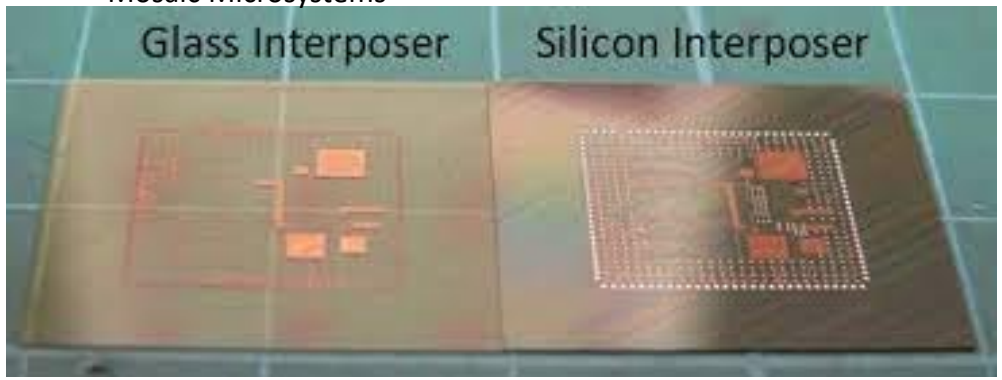
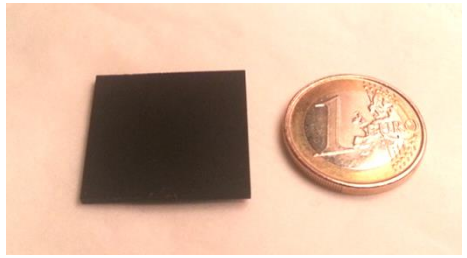
AP Services: Interposers

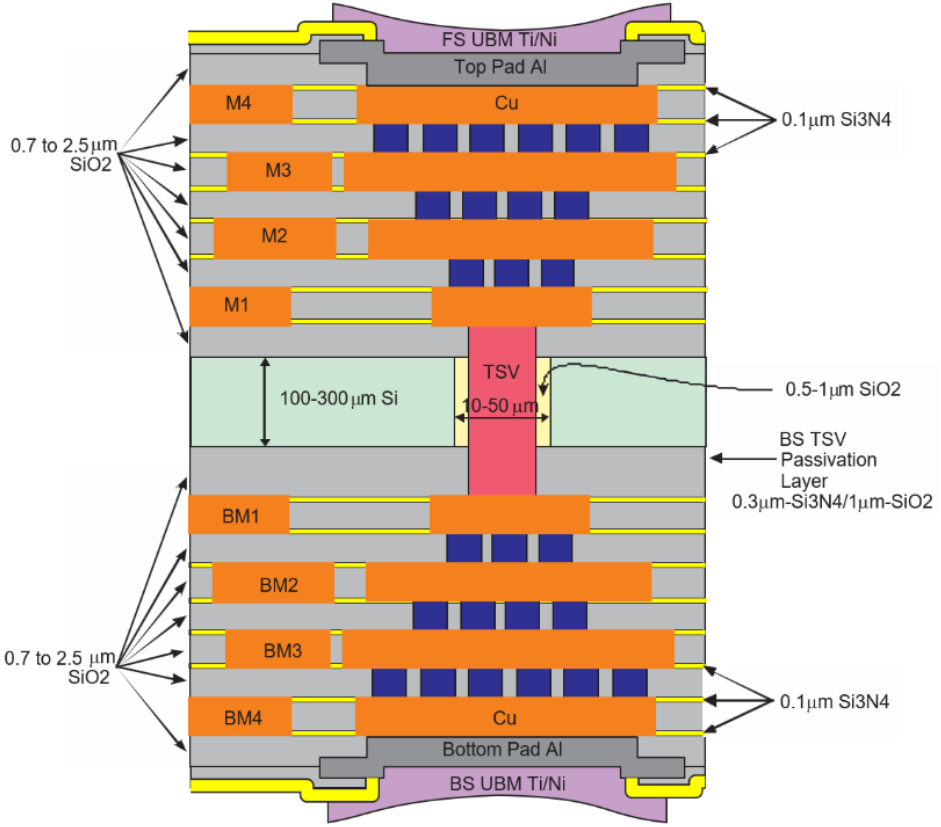
- Bigger, Better, Faster
- Lower Power

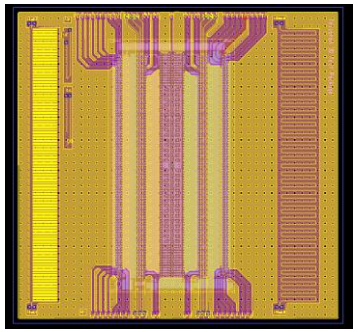
Mosaic Microsystems

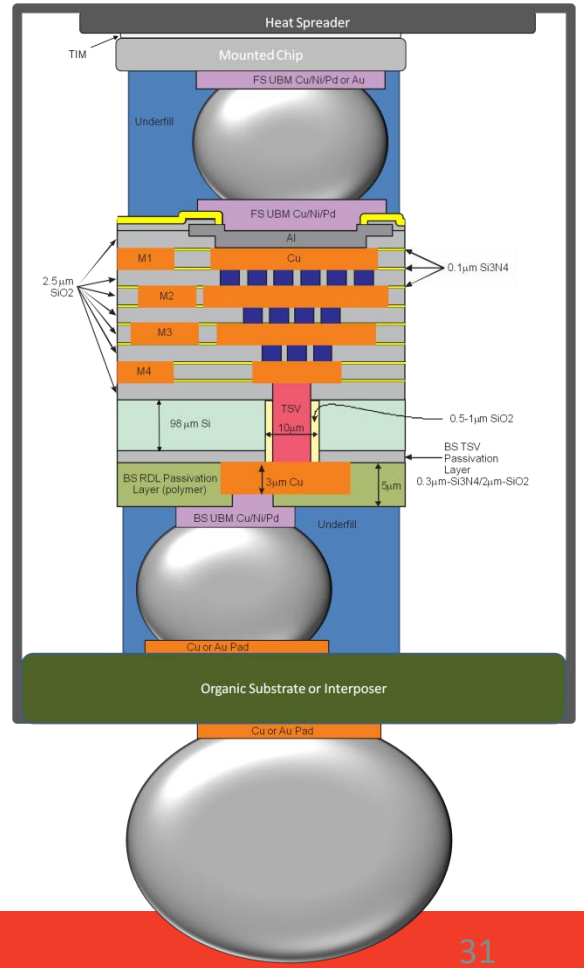




Up to 8 layers of wiring available







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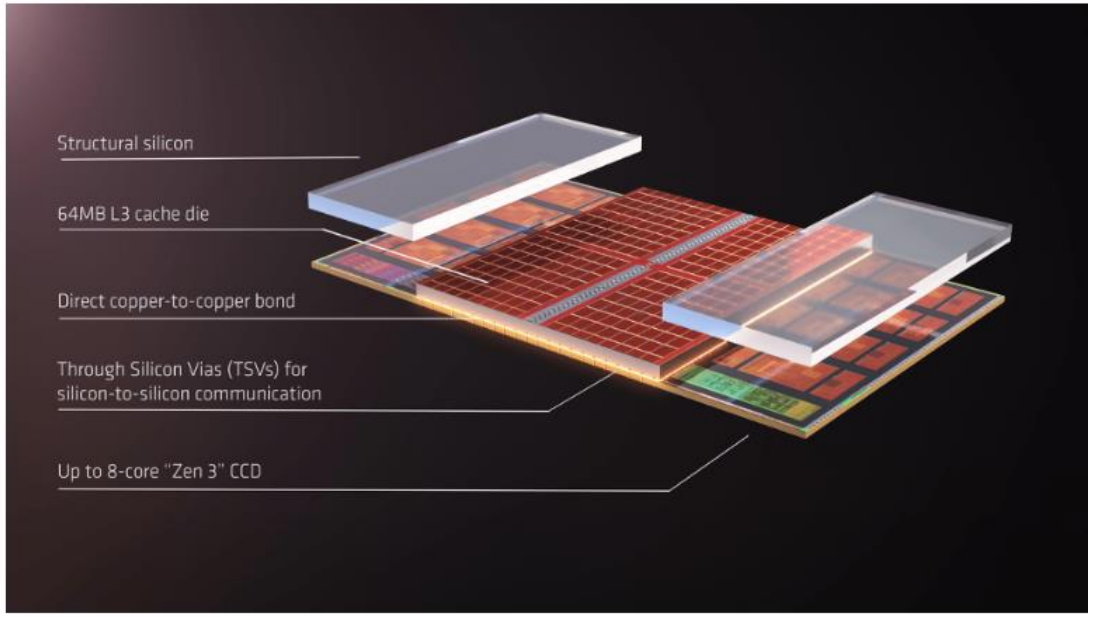
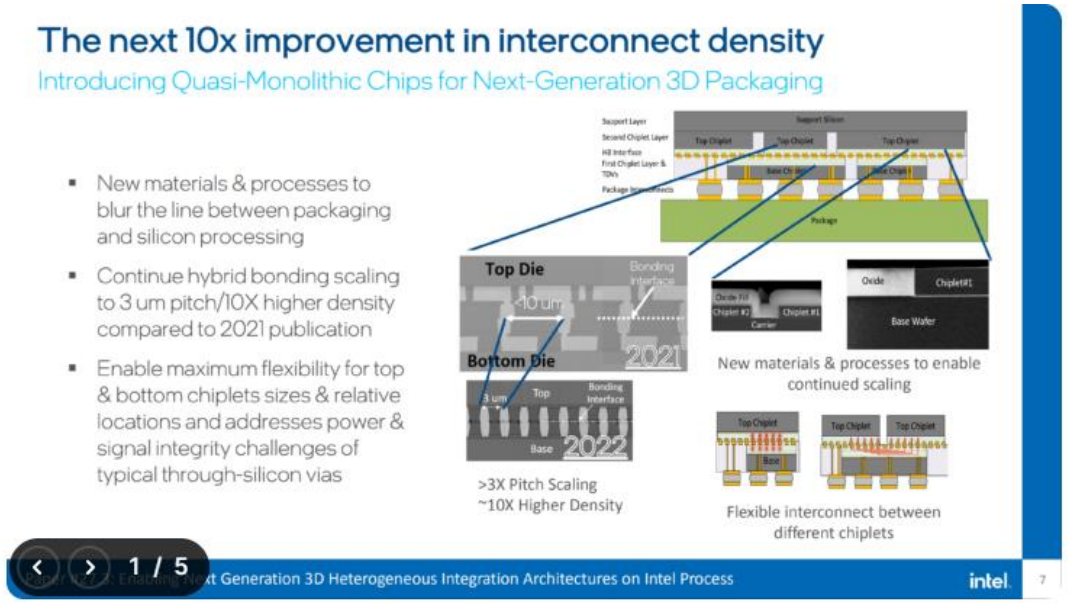
Hybrid Bonding is Enabling Future AI Packaging



AMD's 3D V-Cache using Hybrid Bonding



At IEDM 2022 Intel's Components Research Group is committed to innovating in three targeted areas:

1. 3D Hybrid Bonding of chiplets
2. Super-thin die
3. 2D Materials to fit more transistors onto a chip

Outline

- Heterogeneous Integration – What is it?
- What is the Proper Metric?
- Markets
- What are the Core AP/HI Technologies?
- Maintaining Leadership
- Summary

What are we doing

NHanced Semiconductors Unveils Advanced Packaging Foundry

January 18, 2024 Filippo Di Giovanni

NHanced Semiconductors spearheads a groundbreaking era in semiconductor innovation with the inauguration of its advanced packaging foundry in Indiana.

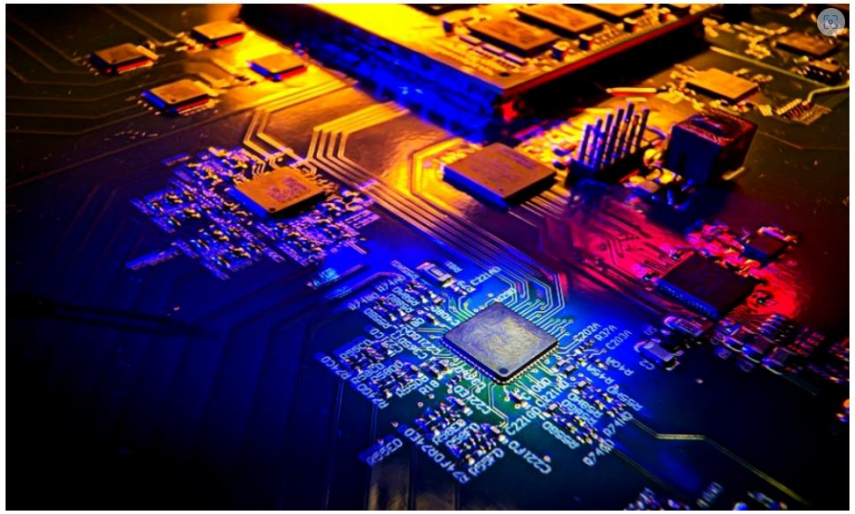
skywater

SkyWater Florida and Deca Technologies Announce $120M DOD Award to Expand Advanced Packaging Capabilities in Osceola County, Florida

January 16, 2024 Daisie Hobson Resource Library 0 Comments

DeSantis recommends $80 Million investment in UF's semiconductor institute

by Caden DeLisa | Jan 26, 2024



Amkor Technology selects Peoria as future home to the largest U.S.-based advanced semiconductor packaging and testing facility

Deal represents $2 billion investment in Peoria, 2,000+ new jobs

Post Date: 11/30/2023 6:03 AM

Peoria, AZ (November 30, 2023) The city of Peoria is finalizing a development agreement with Tempe-based Amkor Technology for the future location of their state-of-the-art advanced semiconductor packaging and testing campus.

"It is no secret that our nation is reshoring its advanced manufacturing industries. We are proud of Peoria's global leadership in this movement, and the significant capital investment and quality jobs that it brings to our community," said Mayor Jason Beck. "This tremendous announcement is a credit to the City Council's commitment to economic development, and staff's hard work and dedication on this project."

While the final details of the development agreement are still being worked out, this announcement will bring 2,000 jobs to Peoria, representing a $2 billion local investment.

Amkor's plans for the Peoria facility will provide high volume, leading-edge technologies for advanced packaging and testing of semiconductors to support critical markets such as high-performance computing, automotive, and communications. The company announced preliminary details of the project earlier today.

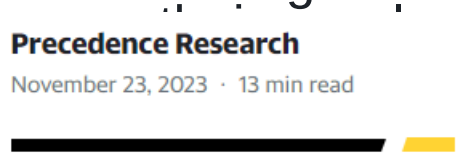
The first phase of the manufacturing plant is targeted for production to begin within the next two to three years.

A final development agreement is scheduled to go before the City Council in early 2024.

NHanced SEMICONDUCTORS

Domestic packaging industry

- **North America is the Fastest Growing Market**
- **Leading regional semiconductor businesses, research institutions, and startups have made North America a hotspot for technological innovation**, which has sparked the creation of cutting-edge packaging methods.
- To remain competitive in the market, the region has a history of making significant investments in R&D for semiconductor technology, which involves the study of packaging methods, materials, and integration procedures. It even features a thriving ecosystem of research facilities, equipment manufacturers, semiconductor companies, and design studios. **New packaging solutions may be developed and implemented quickly in this collaborative setting, which also speeds up innovation.**
- More complex semiconductor packaging solutions are required due to the rising demand for high-tech electronics such as smartphones, IoT devices, automotive electronics, and data center equipment. To meet these needs, **North American businesses have been leading the way.** Particularly in the wake of global supply chain disruptions, the significance of a strong and resilient semiconductor supply chain has come to light. Businesses in North America have made investments in plans to i chain capabilities.



NHanced SEMICONDUCTORS

PRECEDENCE RESEARCH

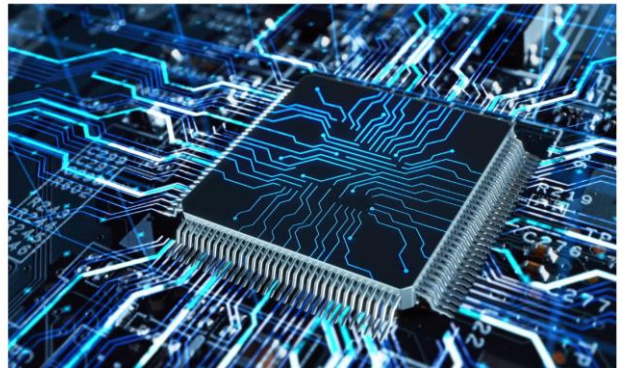
- Increase advanced packaging facility capacity in the United States Industry analysts expect that there will be **29 new fab construction projects started by the end of 2022.** These 29 fabs are estimated to produce up to 14.5 million wafers per year (in 300 mm equivalents).38 This increased wafer fabrication capacity necessitates more advanced packaging capacity in particular, and ATP capacity more generally, to maintain processing volumes. Current assembly, test and packaging (ATP) capital expenditure investment levels will need to be sustained or expanded so that OSATs, IDMs, and foundries have the capacity in place to assemble, test, and package the increased wafer fabrication capacity as it comes on line. **OSATs, IDMs, and foundries are all contemplating new construction of ATP facilities to meet this greater demand**, and the United States should provide incentives to encourage firms to establish or expand ATP capacity domestically.

University and Industry Partnerships

Florida Semiconductor Institute to help lead state in critical chips sector

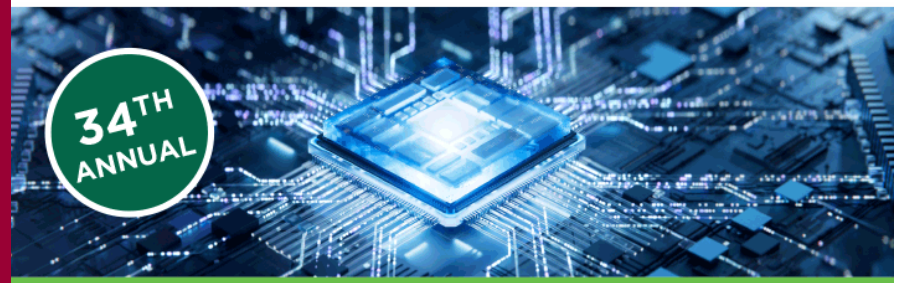
In Department of Computer and Information Science and Engineering, Department of Electrical and Computer Engineering, ICYMI, News / October 5, 2023 / By Karen Dooley

Penn State leads semiconductor packaging, heterogeneous integration center



ASU Arizona State University

Advanced Semiconductor Packaging



ELECTRONICS PACKAGING SYMPOSIUM

SEPTEMBER 6-7, 2023 • ALBANY NANOTECH COMPLEX

Presented by: IEEC, Binghamton University • CAMM, Binghamton University • GE Global Research • IBM Research

NHanced SEMICONDUCTORS

Outline

- Heterogeneous Integration – What is it?
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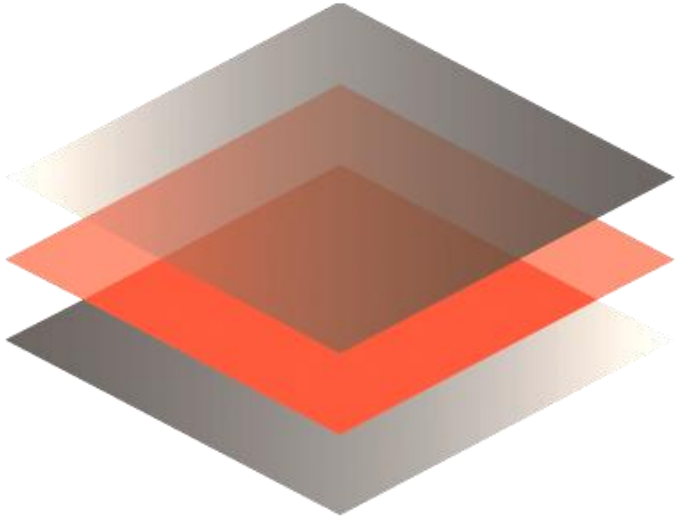
Summary

- Chiplet integration is the lowest cost method to create a packaging system in a timely manner, which enables near monolithic interconnects.
- Chiplet ecosystem is changing from solder → hybrid bonding. Standards are required to support physical interoperability.
- The Achilles heel for making 3DHI more prevalent is developing better assembly methods, especially for D2W hybrid bonding.
- Better methods need to be developed to handle thin dies for KGD testing.
- Another major technical challenge for 3DHI is thermal management. This will require the development of improved thermal dissipation technologies.
- A better metric to characterize 3DHI performance needs to be created. Moore's Law is no longer appropriate.
- Developing strong University and Industry partnerships is imperative to maintain AP/Hi domestic leadership.
- Future domestic opportunities are for high mix, low volumes.
- Customers want domestic AP/HI capabilities.

Thank You



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