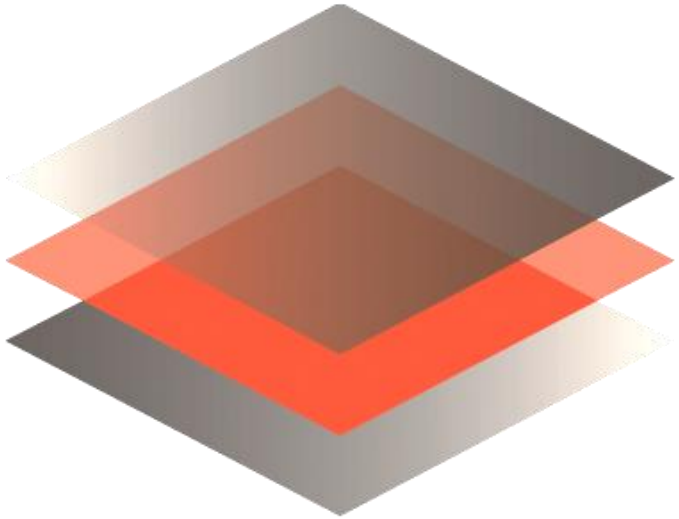
NHanced Semiconductors

Hybrid Bonding: Tools and Techniques Enabling Advanced Packaging



June 23, 2024

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Effective End of Moore's Law

Moore's Law was first and foremost a statement about economics. We could shrink transistors and build more of them for about the same cost.

- This has been the basic premise of the semiconductor industry for 50 years and was true up until the last few years.
- Today we can indeed shrink transistors further, but the cost per transistor no longer declines.

  We can get something a little more compact

  - Perhaps a little less power
  - But we pay more for these features now.

What Does This Mean?

The semiconductor industry is about to undergo a sea change.

- New ways of accomplishing Moore's law economics and performance are needed.
  - The industry is now looking to use advanced packaging to drive future semiconductors.
    - Better Cost
    - Better Performance
    - Better SWaP

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Vision of the Future

A new semiconductor industry paradigm is evolving…

Foundry 2.0 –

A Finishing Foundry that takes the standardized building blocks from traditional semiconductor manufacturers and uses advanced packaging and additive manufacturing to create highly customized components with superior performance targeting small and medium sized markets.

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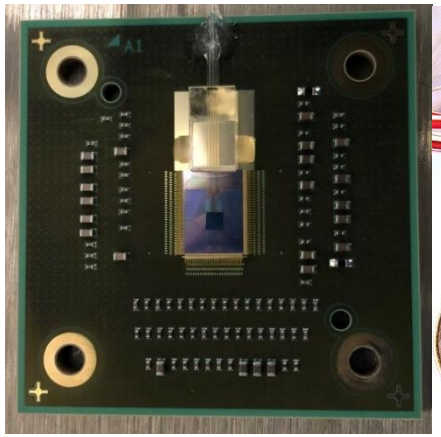
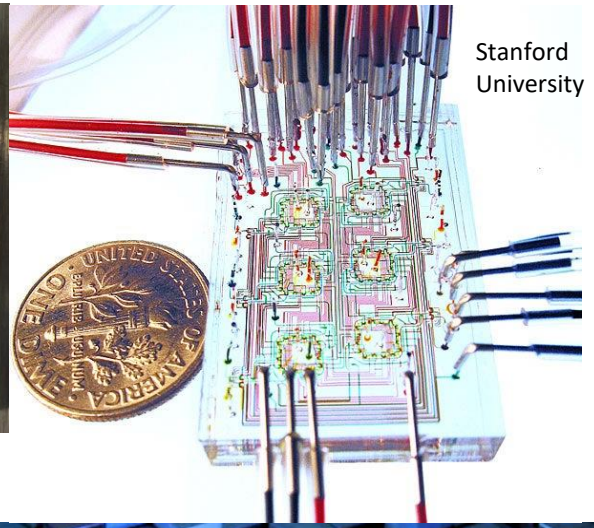
Foundry 1.0

- Current semiconductor business has been focused on driving smaller transistors.
  - High development cost
  - High capital cost
  - Long development times
  - Expensive design tools
  - High risk
- Twilight of Moore's Law

Foundry 2.0

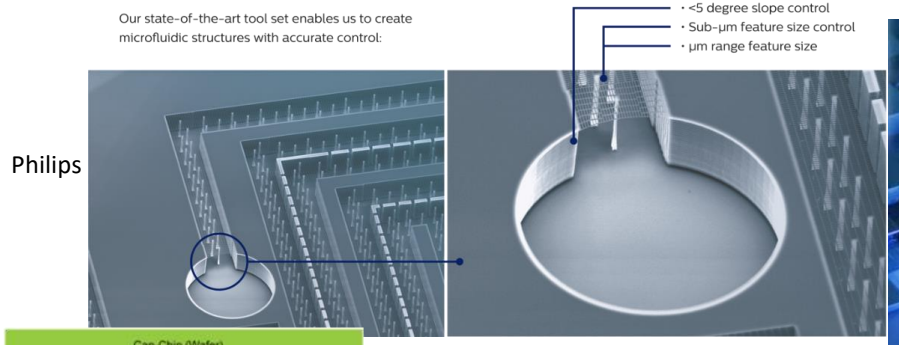
- System solution focus
  - Best of class components
- Relies on Advanced Packaging (AP) and Chiplets
  - Heterogenous integration
  - Photonics
  - MEMS
  - RF
- Advantages
  - Low development cost
  - Low capital cost
  - Short development times
  - Inexpensive design tools
  - Low risk





Stanford University

Philips



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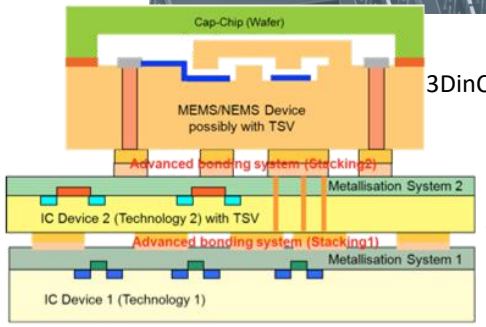

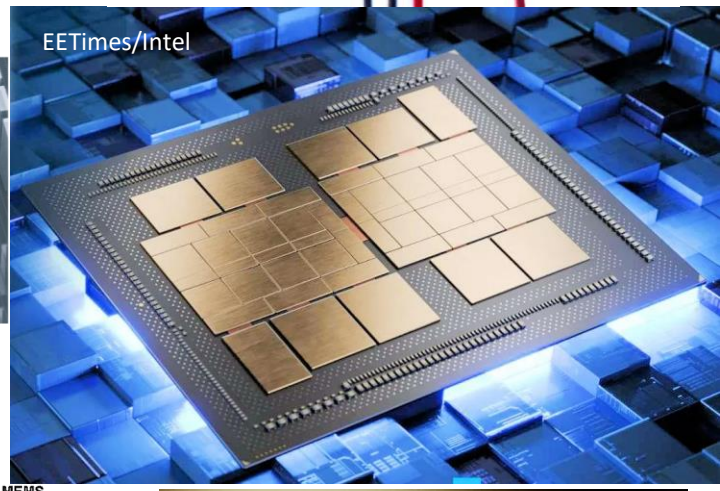

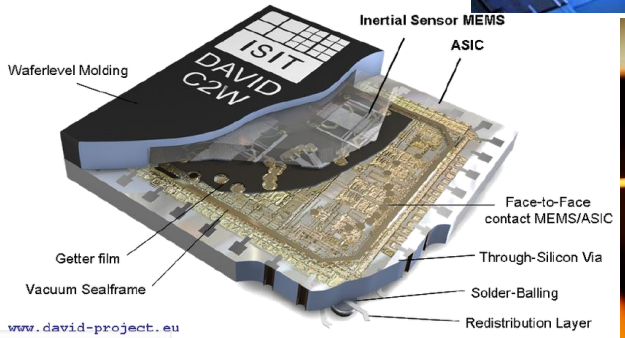

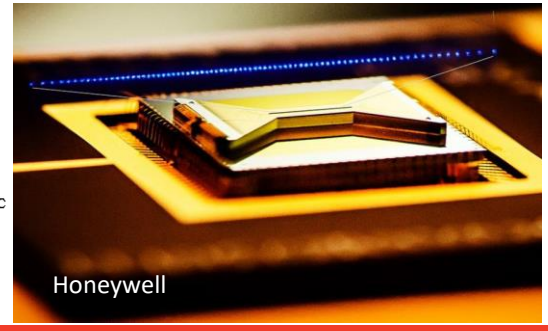

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Foundry 2.0 Opportunity

- There are no de facto winners
  - Intel, AMD, Xilinx, Marvell, -- Currently IDM driven but nascent
- Low capital costs
  - More than an order of magnitude lower capital costs
- Supports low and medium volume flows – High mix fabrication
  - USG, startups, large swath of industry
    - More cost effective
  - Competition is FPGAs
    - 10x to 50x lower component cost
- IP centric
  - Knowledge based value
- Phased approach works well
- Complement to Foundry 1.0
  - Partnering
    - Customers, Capital, Pile-on

Changes the Market
Low-Volume
High-Mix Manufacturing

Why Are We Headed To Low Volume Manufacturing?

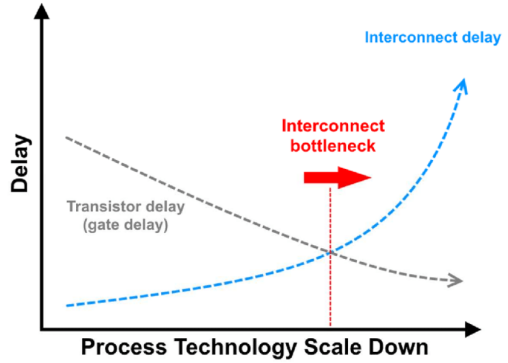
- Transistor cost is increasing
  - To reduce cost, we need to sell the consumer fewer transistors
  - Most semiconductor devices have the kitchen sink
    - NRE is high so we can't target markets
- Chiplets offer reuse – effectively $0 NRE
- Advanced packaging NREs run ~100x less cost than lead edge node NREs
- Chiplet to chiplet power and delay is competitive with on die
- Chiplets can target markets – use only necessary transistors

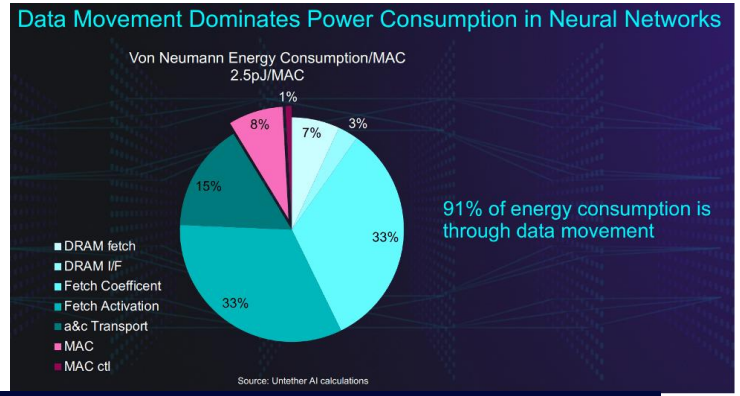
→ Low NRE → Niche Market → Fewer Transistors → Lower Cost Composite Device

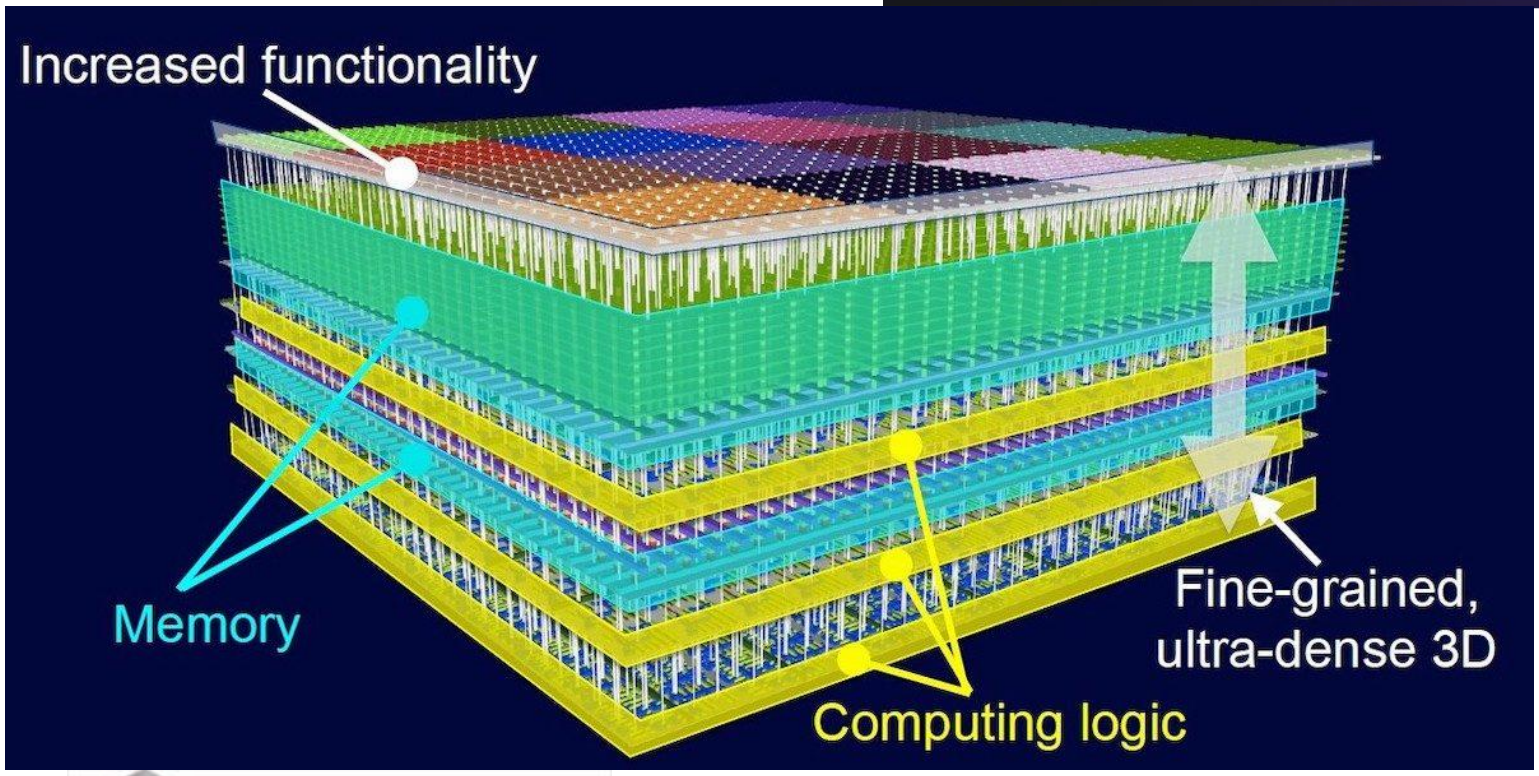
Moore's Law for the Next Decade

Fundamentals: Wiring (Metallization)

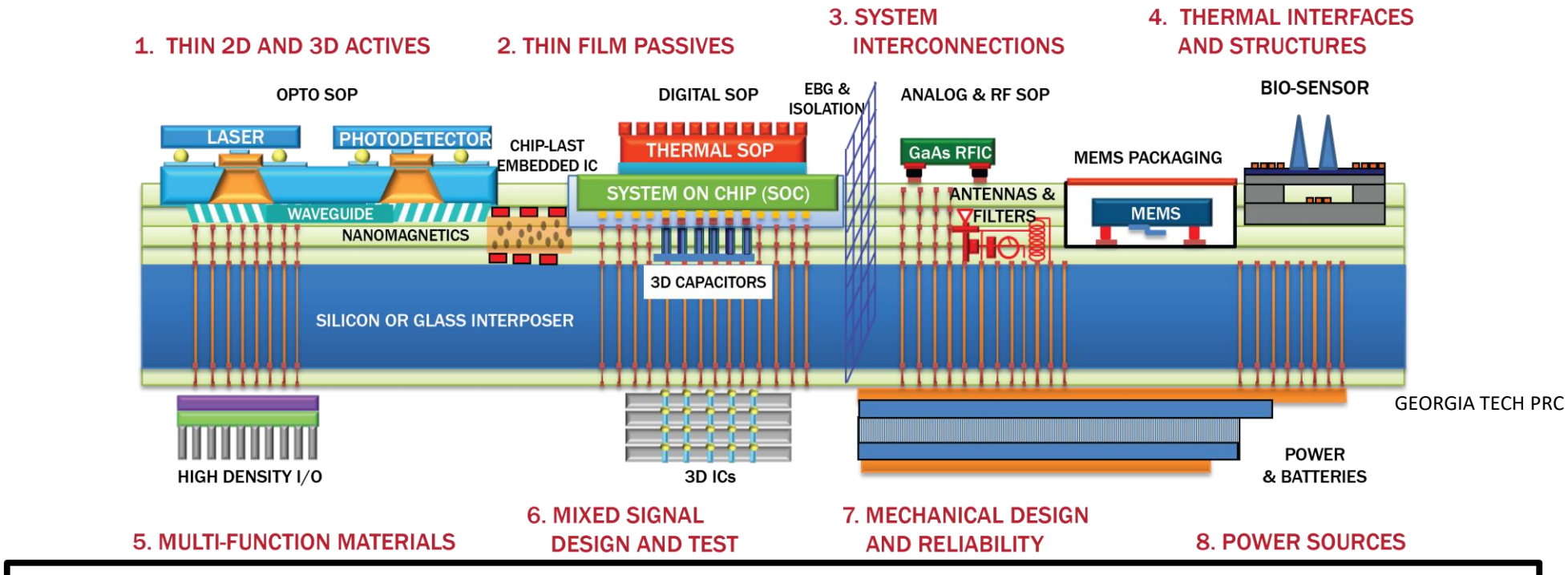
- Wire length controls the delay
  - Span of control
- Accounts for majority of power usage
  - Memory fetch







Fundamentals: More Than Moore Technologies



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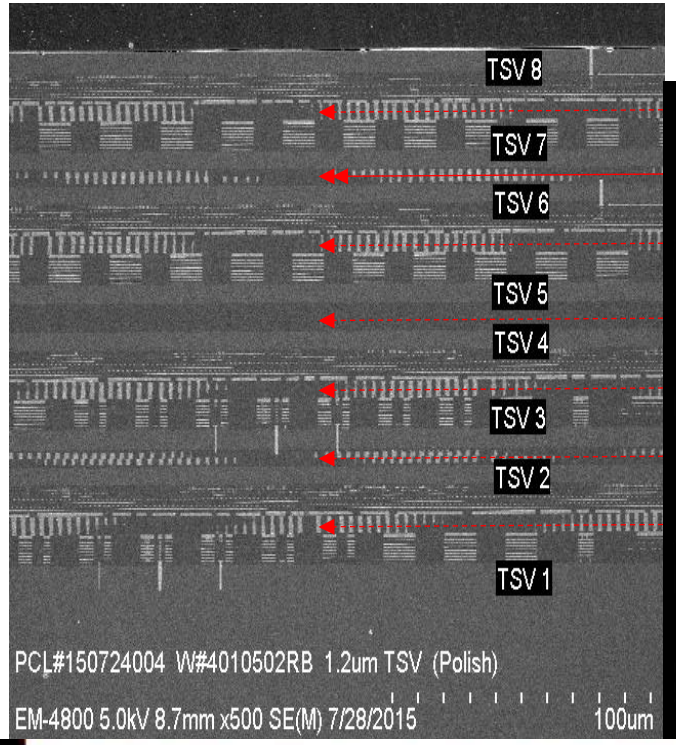
AP Elements: Bonding

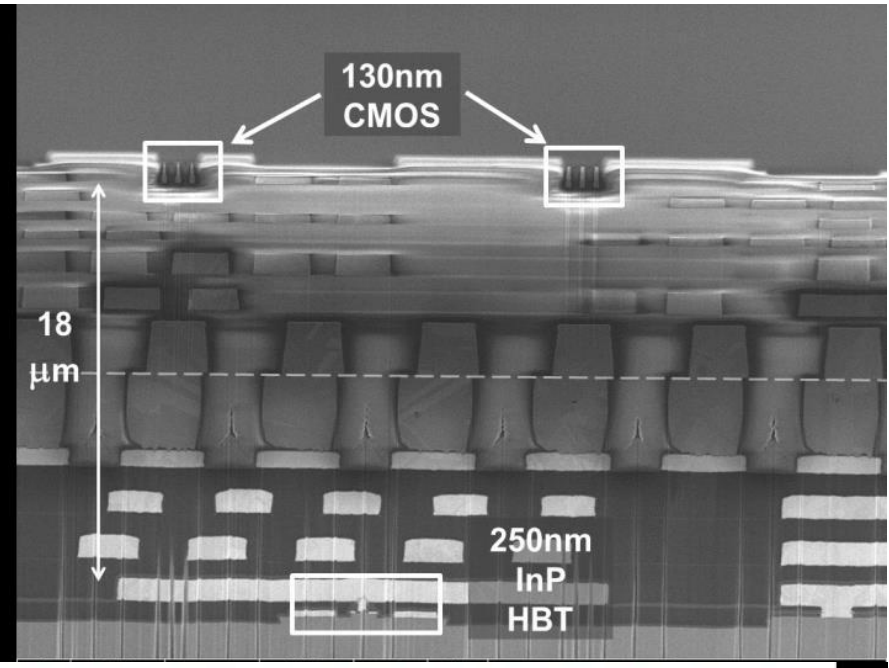
Millimeters ⇨ Microns

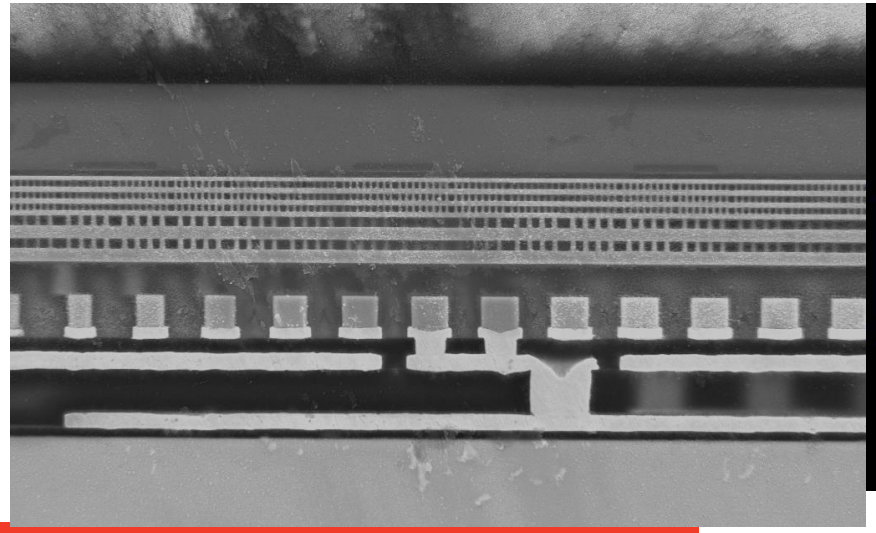
- No ESD requirement on I/O
- TCB
- Oxide
- Hybrid bonding
  - Cu
  - Ni

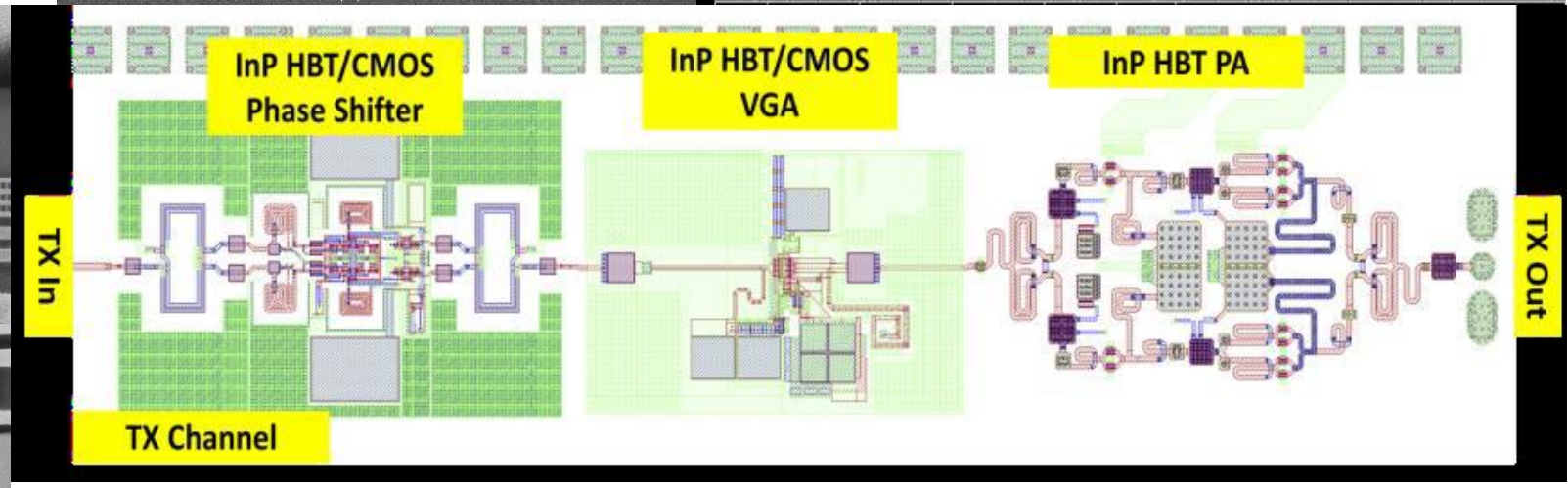
Mixed Materials

Best of Class









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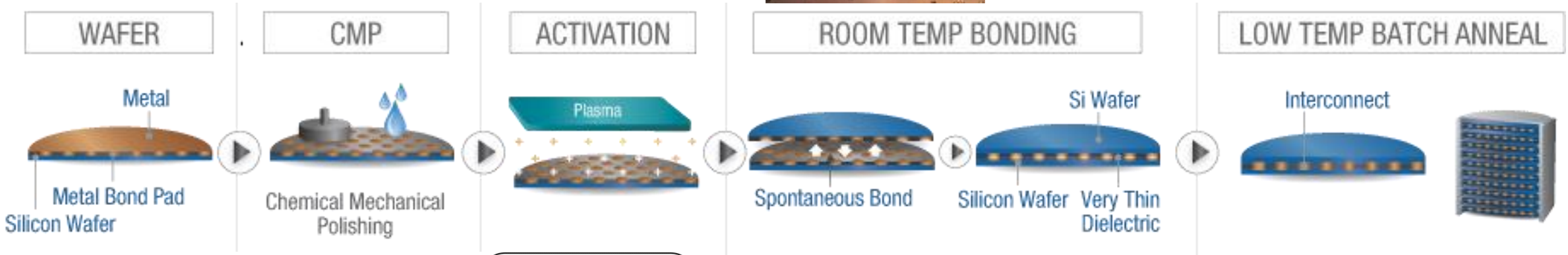
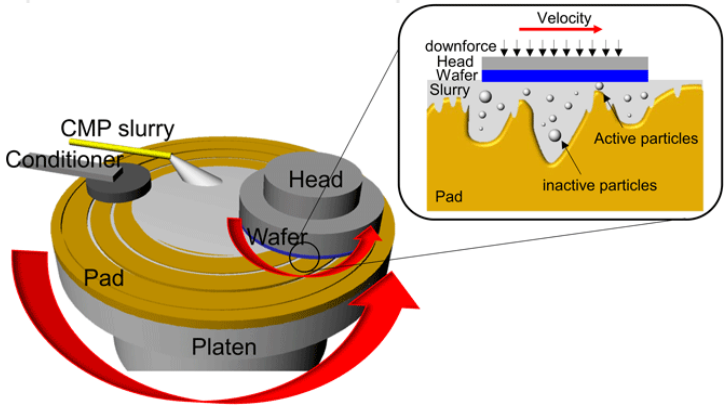
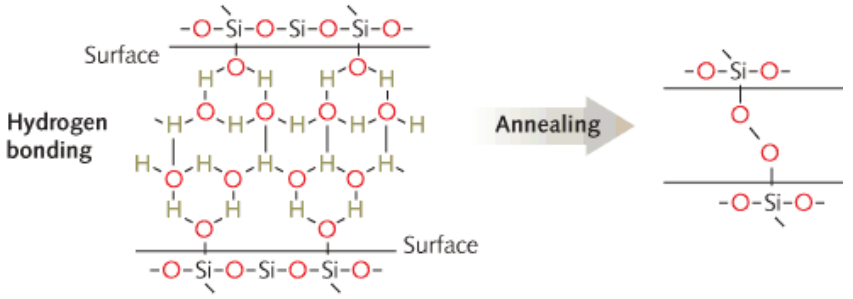
DBI®: Low Temperature Hybrid Bonding Process







Jihoon Seo / Materials Research Society

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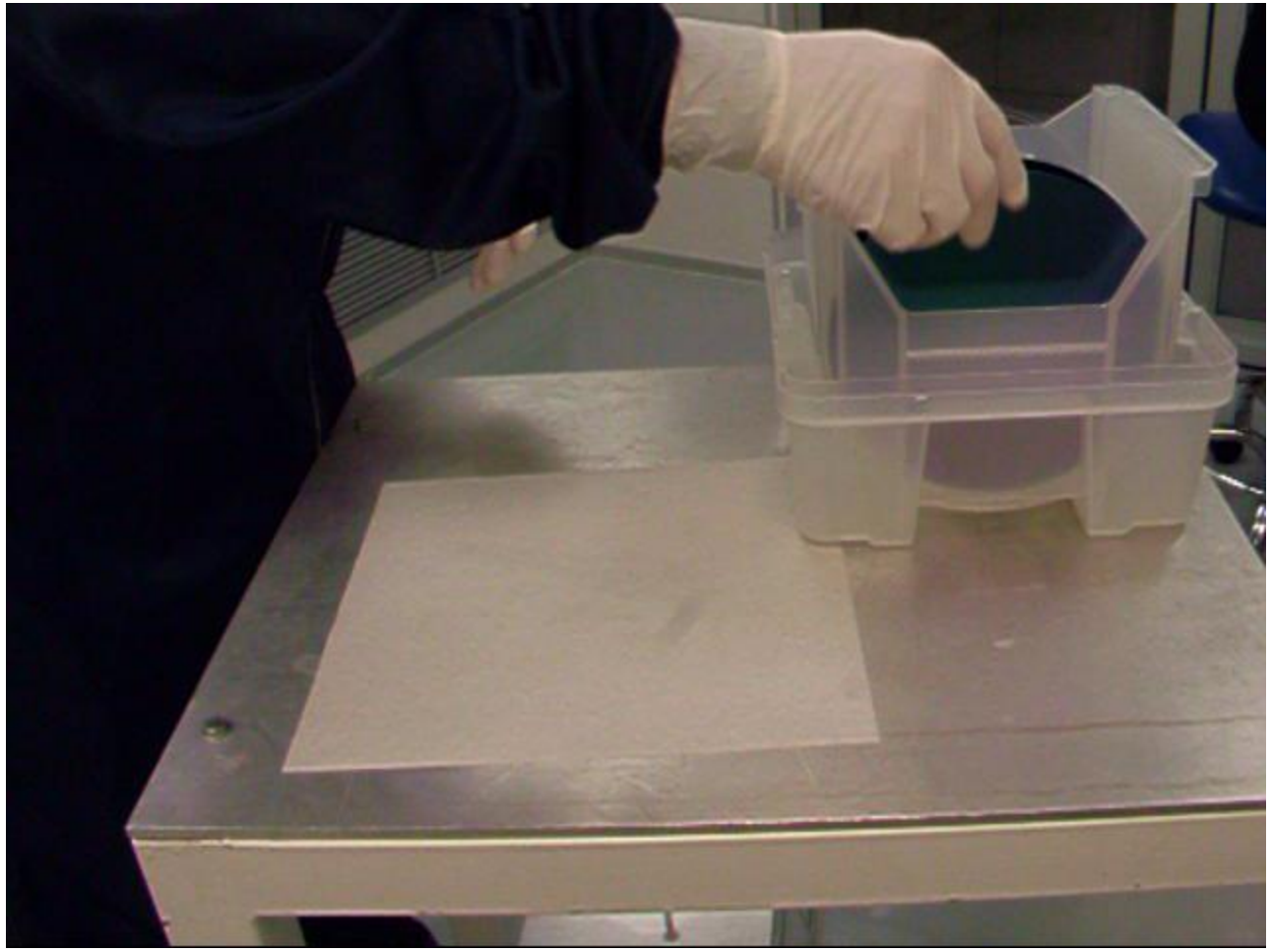
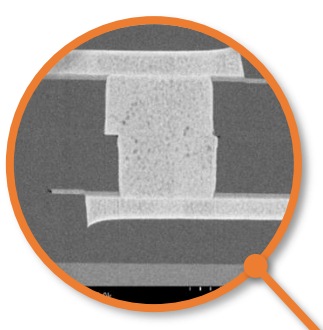
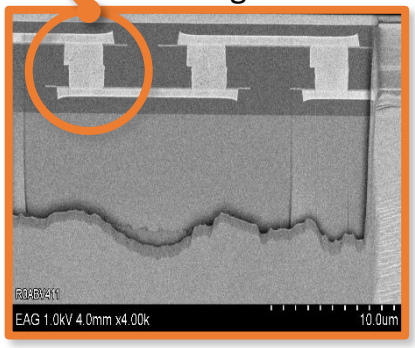
Bonding in Action



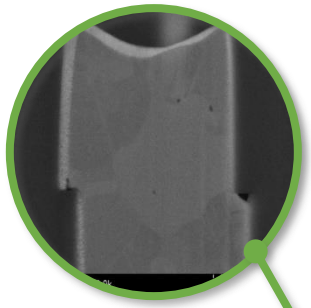
Hybrid Bonding Interconnect Pitch Scaling



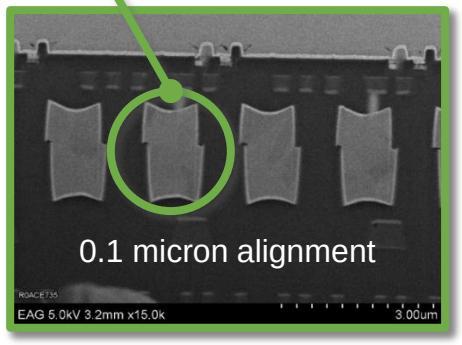
Cu/SiN DBI® Hybrid Bonding



10 µm DBI® pitch, 300℃

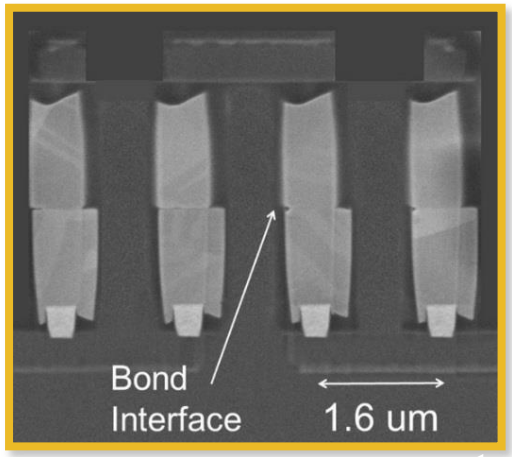


Cu/SiO DBI® Hybrid Bonding



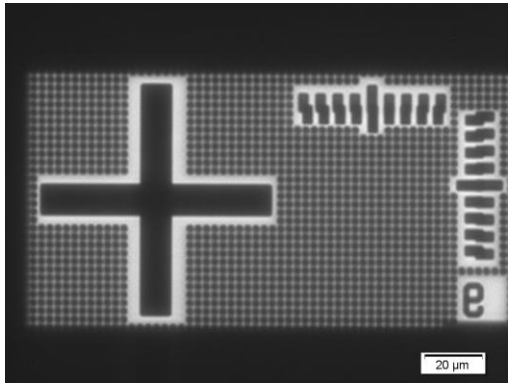
1.9 µm DBI® pitch, 300℃

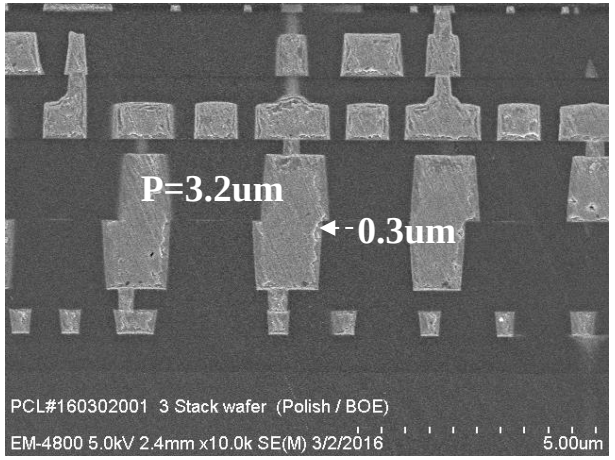
Scalable To < 1um Pitch
0.8um Pitch Demonstrated



1.6 µm DBI® pitch, 300℃

- WtoW 3sigma < ±1um misalign performance
- DtoW 3sigma < ±200nm misalign performance
- Production Minimum pitch = 2.44um
- Best alignment is achieved with face-to-face bonding





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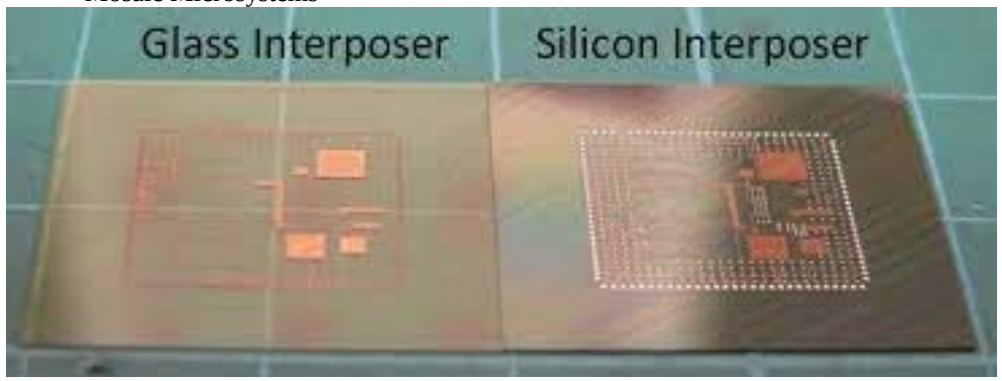
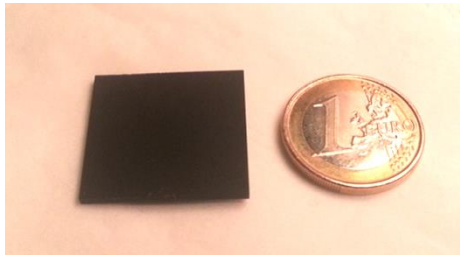
AP Elements: Interposers

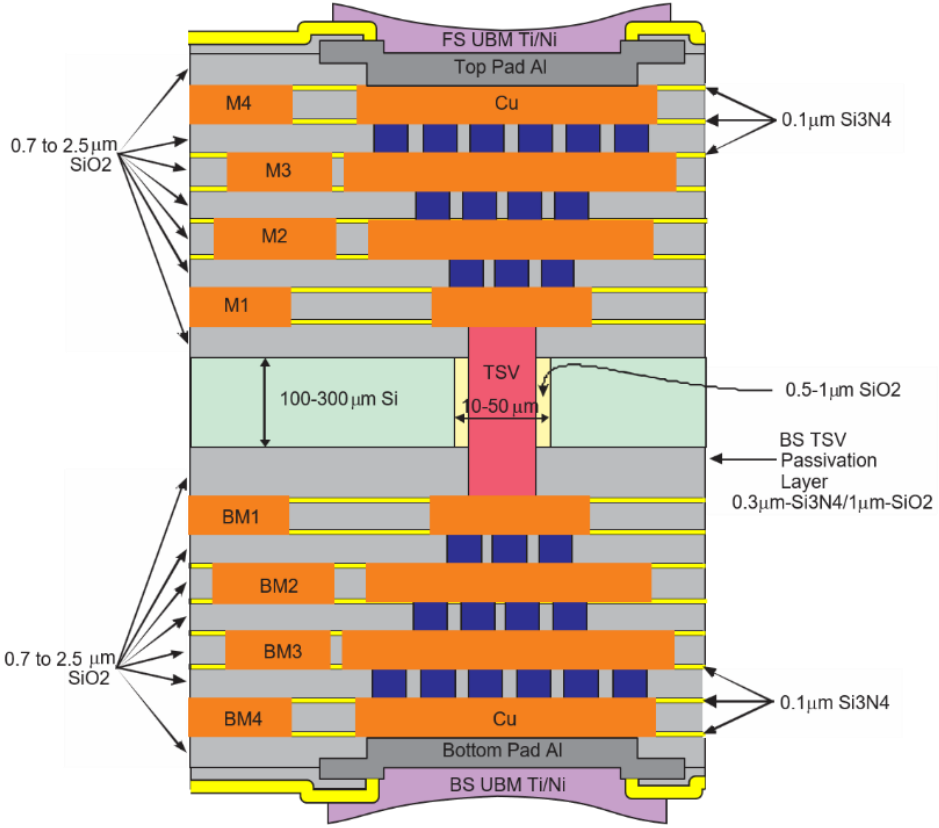
- Bigger, Better, Faster
- Lower Power

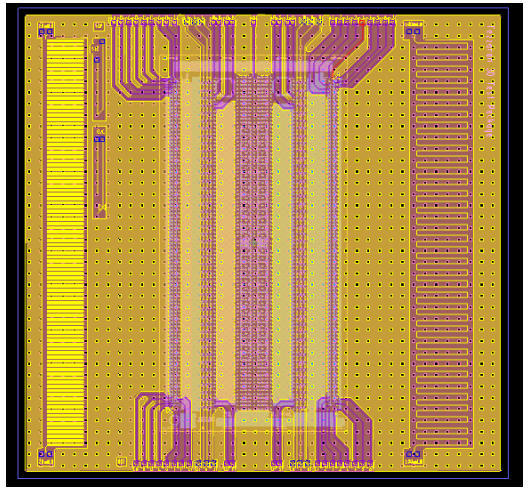
Mosaic Microsystems

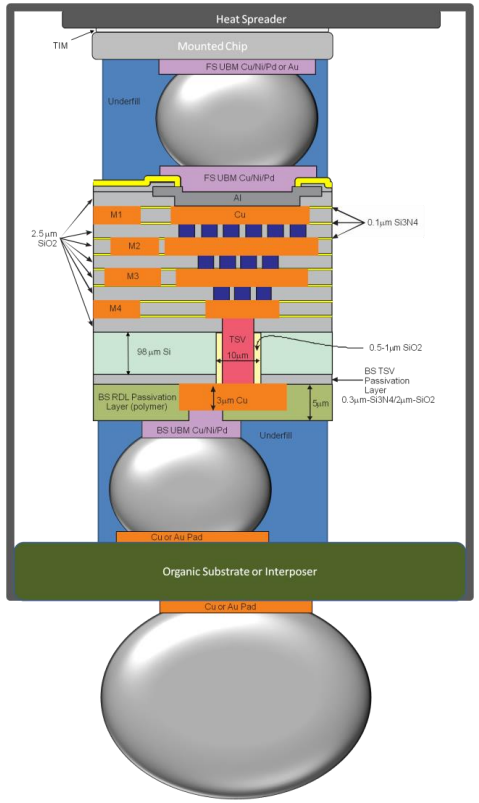




Up to 8 layers of wiring available







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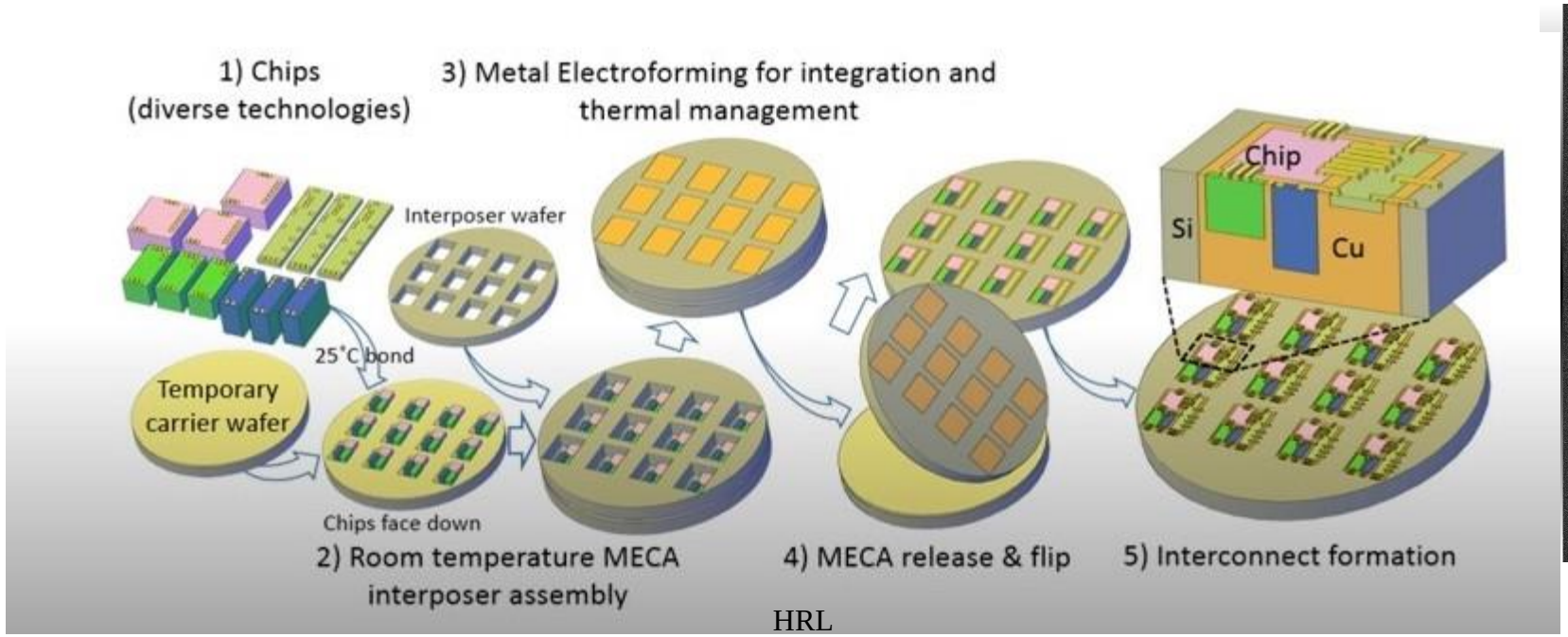
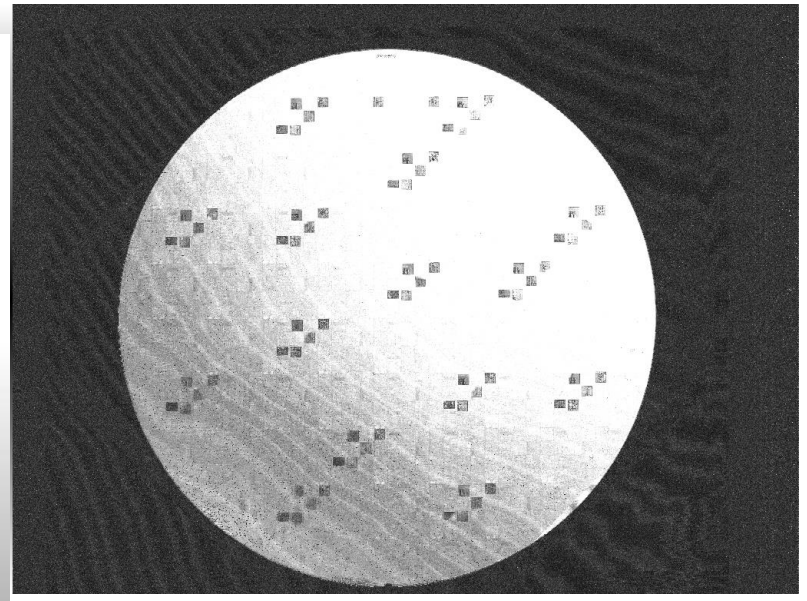
AP Elements: Wafer Reconstitution

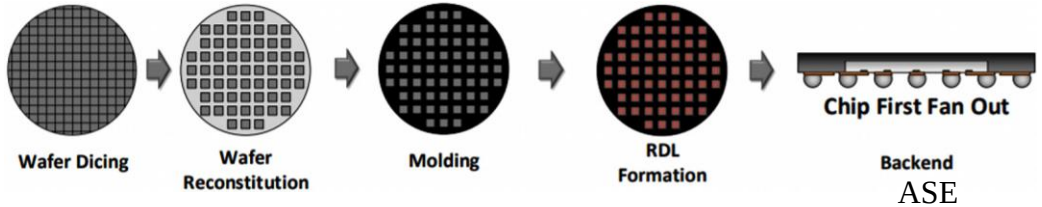


HRL



Wafer reconstruction and adaptative substrates provide additional flexibility and next level packaging alternatives.

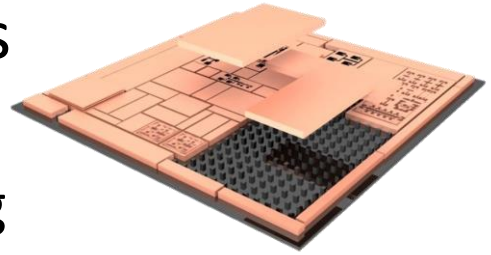
DECA Technologies

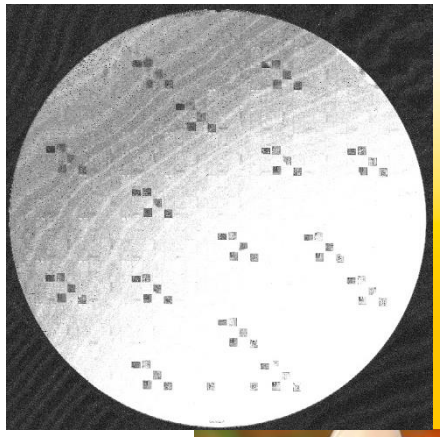


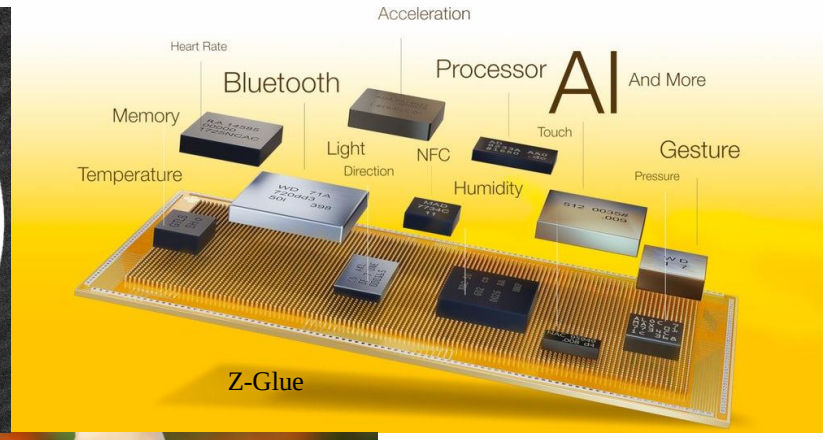
ASE

AP Elements: Chiplets

- The Promise of Chiplets
  … Just Like Legos®:
  - Best of Class Everything
  - Easy retargeting
  - Lower risk
  - IP reuse
  - Lower cost

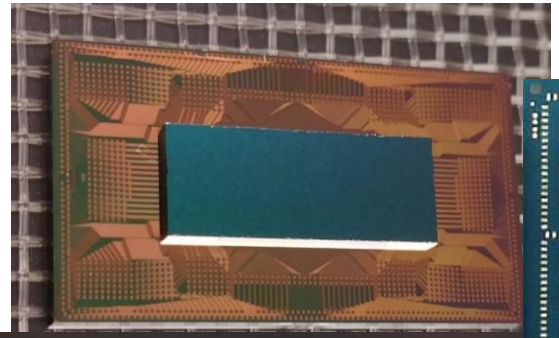


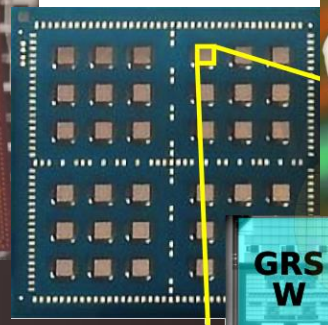


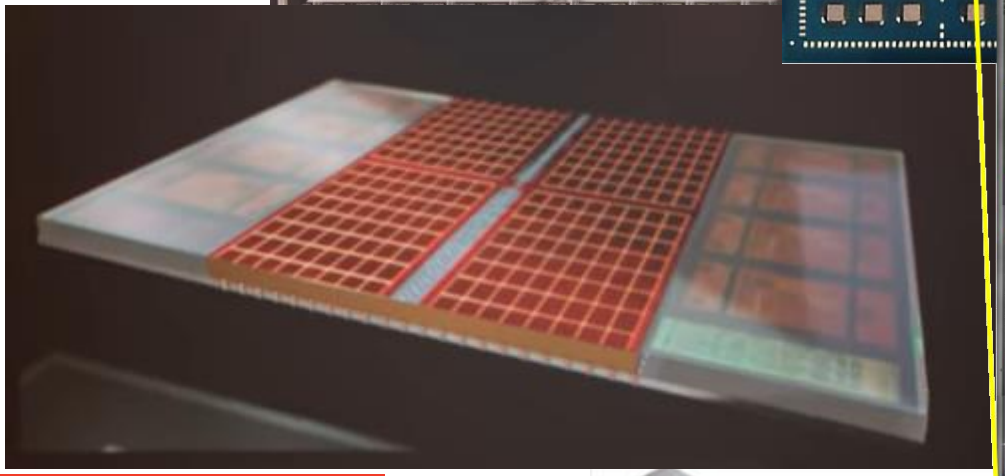


Z-Glue

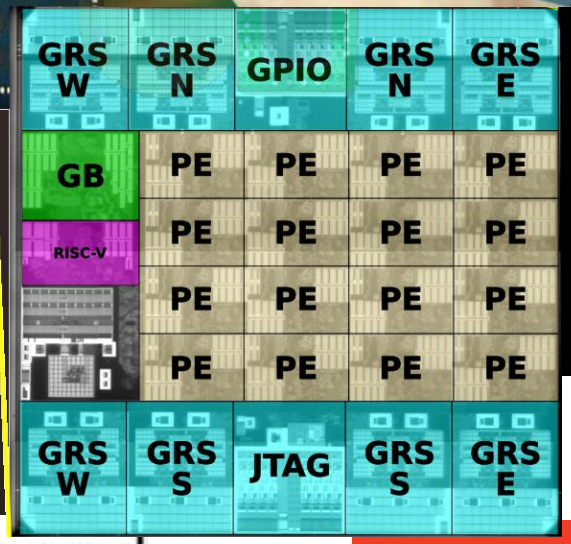
Intel







AMD



Intel

nVidia

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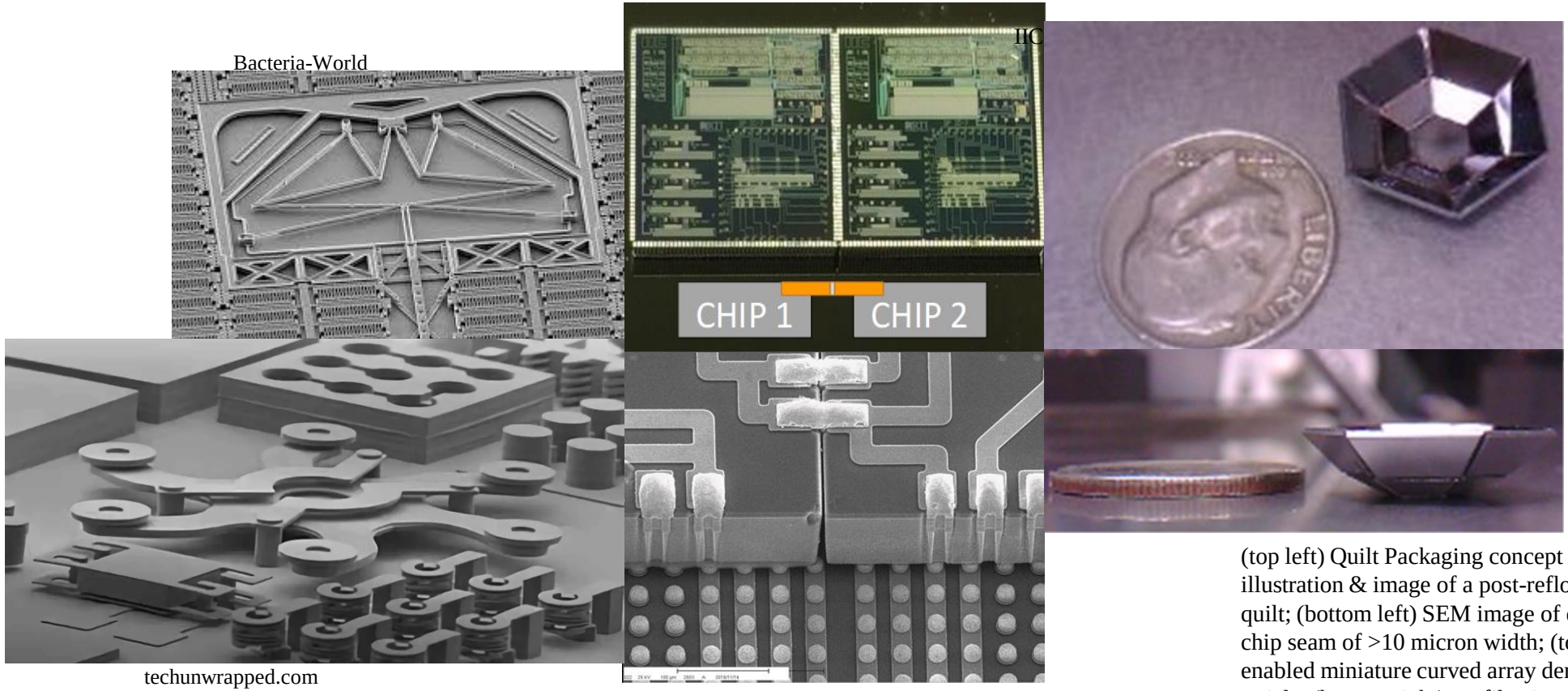
AP Elements: 2.5/3D Micro-Connections

MEMS + Precision Electronics



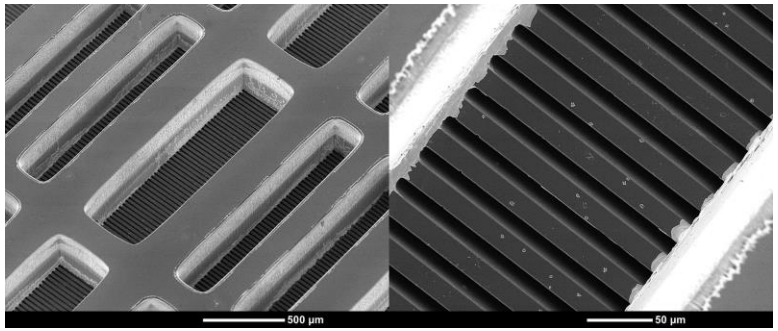
(top left) Quilt Packaging concept cross-section illustration & image of a post-reflowed QP CMOS quilt; (bottom left) SEM image of quilted chip-to-chip seam of >10 micron width; (top right) QP-enabled miniature curved array demonstration article; (bottom right) profile view of QP-enabled miniature curved array.

AP Elements: Microfluidics and Cooling

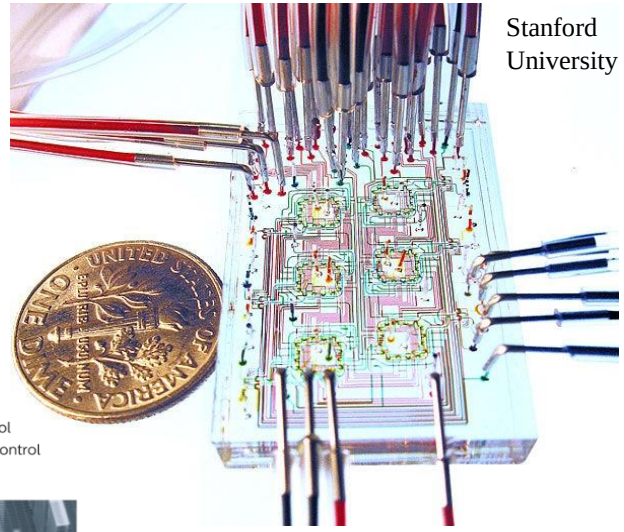
Chip Scale Cooling

For Ultra-Dense Electronics

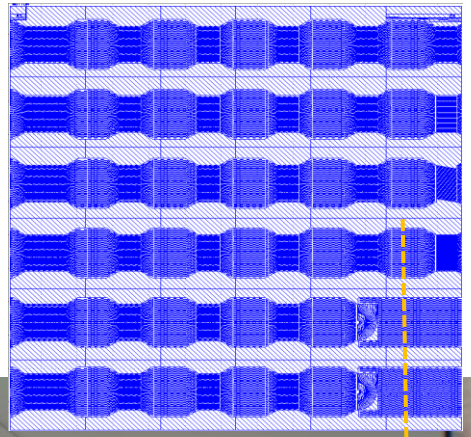
Purdue

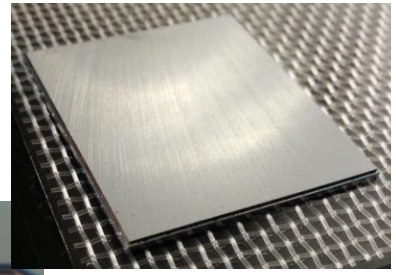


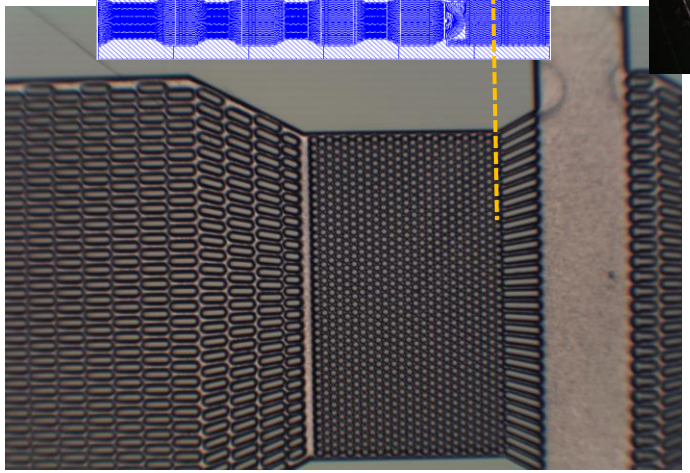
Biology + Electronics



Stanford University

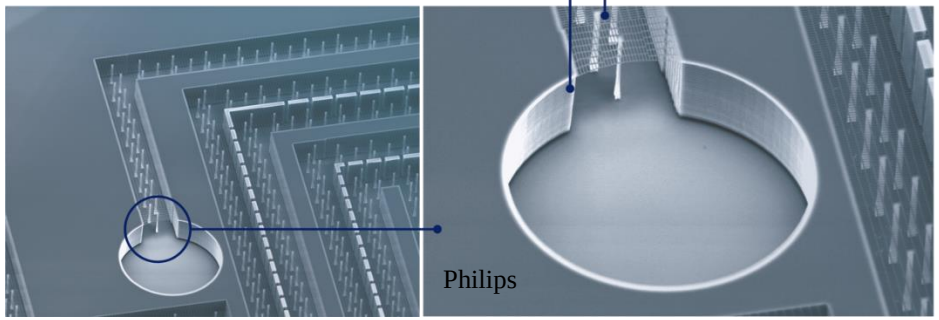






Our state-of-the-art tool set enables us to create microfluidic structures with accurate control:

- <5 degree slope control
- Sub-µm feature size control
- µm range feature size



Philips

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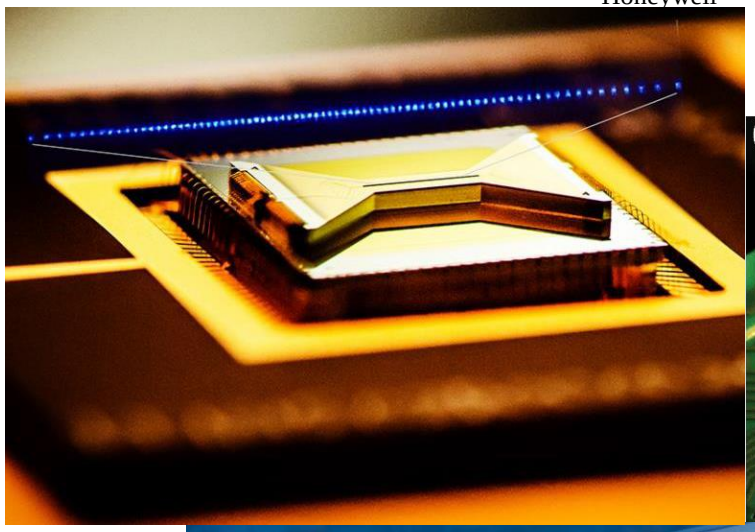
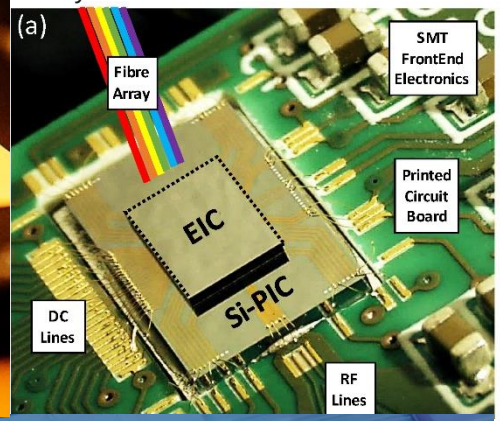
AP Drivers: Photonics & Quantum

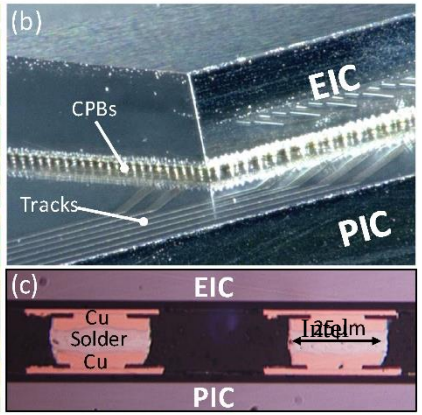
- I/O
  - Tb/s, <<100fJ/b
    - SiP 500ff I/O Load
    - 2.5D 25ff I/O Load
    - 3D 3ff I/O Load
- Processing
  - “Quantum Leaps”

Honeywell

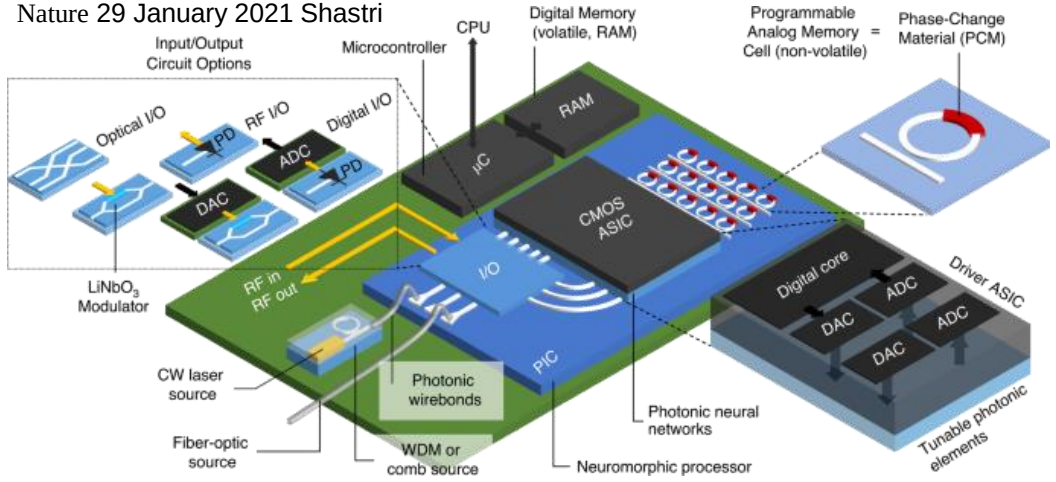


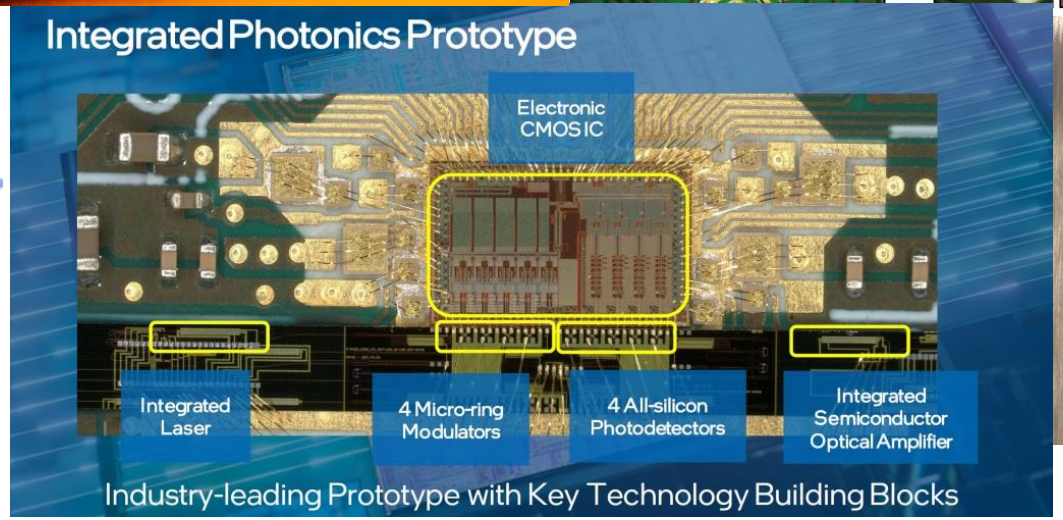
Tyndall National Institute Carroll et al

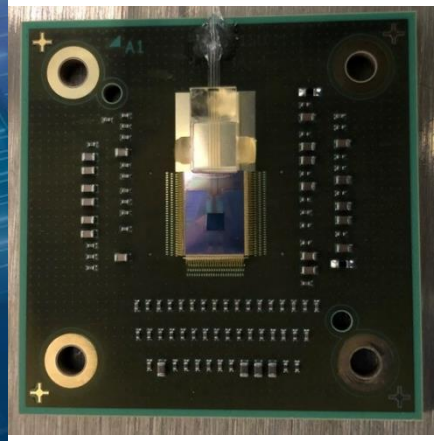




Nature 29 January 2021 Shastri





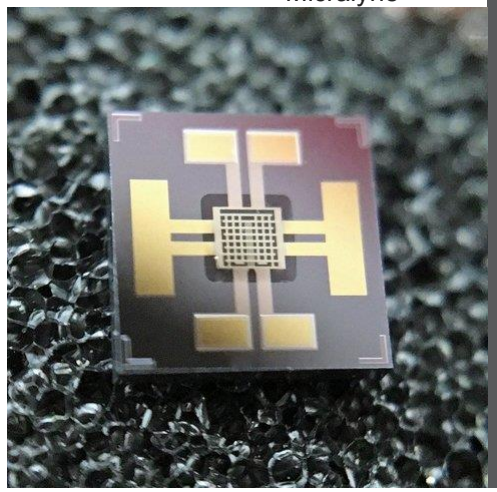


NHanced SEMICONDUCTORS

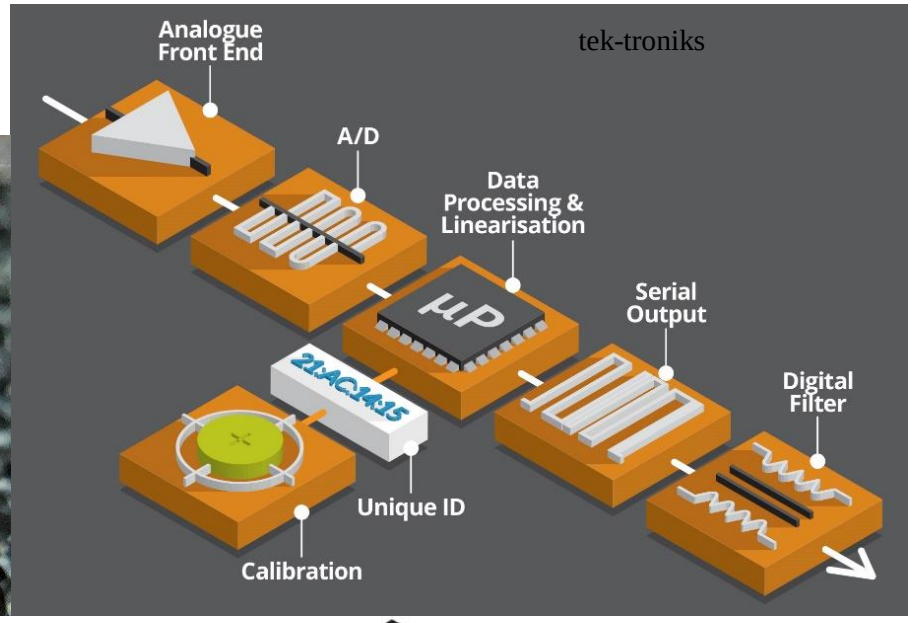
AP Drivers: Intelligent Sensors and Edge Compute

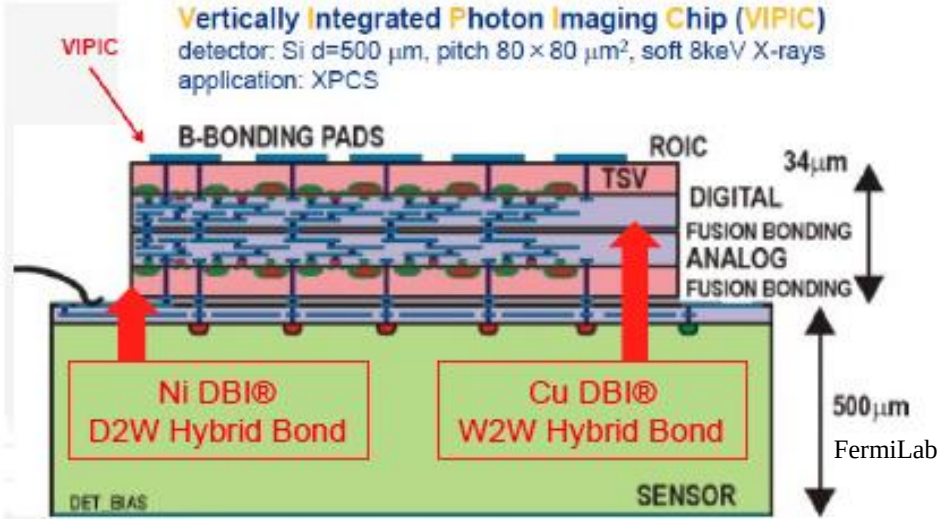
- Communication is limited
  - Data movement costs power
  - Data movement costs time
  - Data movement costs money
  - You can't aways "phone-home"

Micralyne

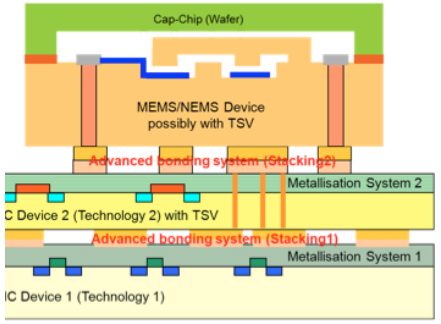


tek-troniks

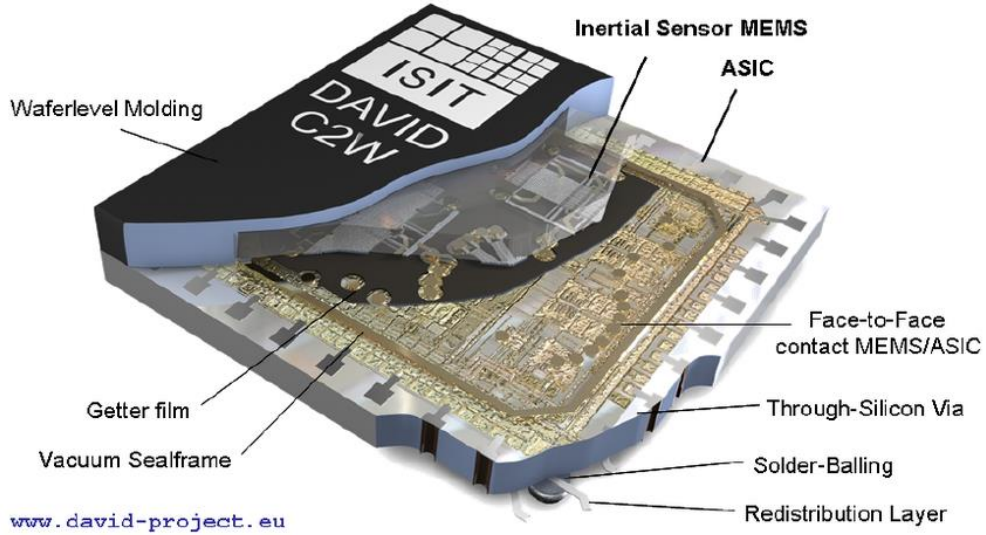




FermiLab



3DinCites

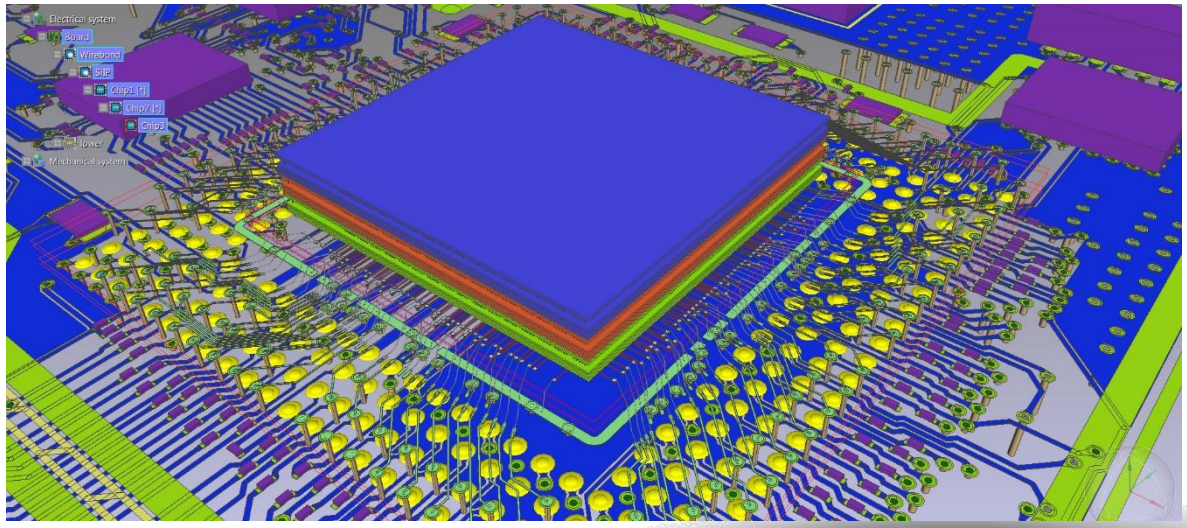


NHanced SEMICONDUCTORS

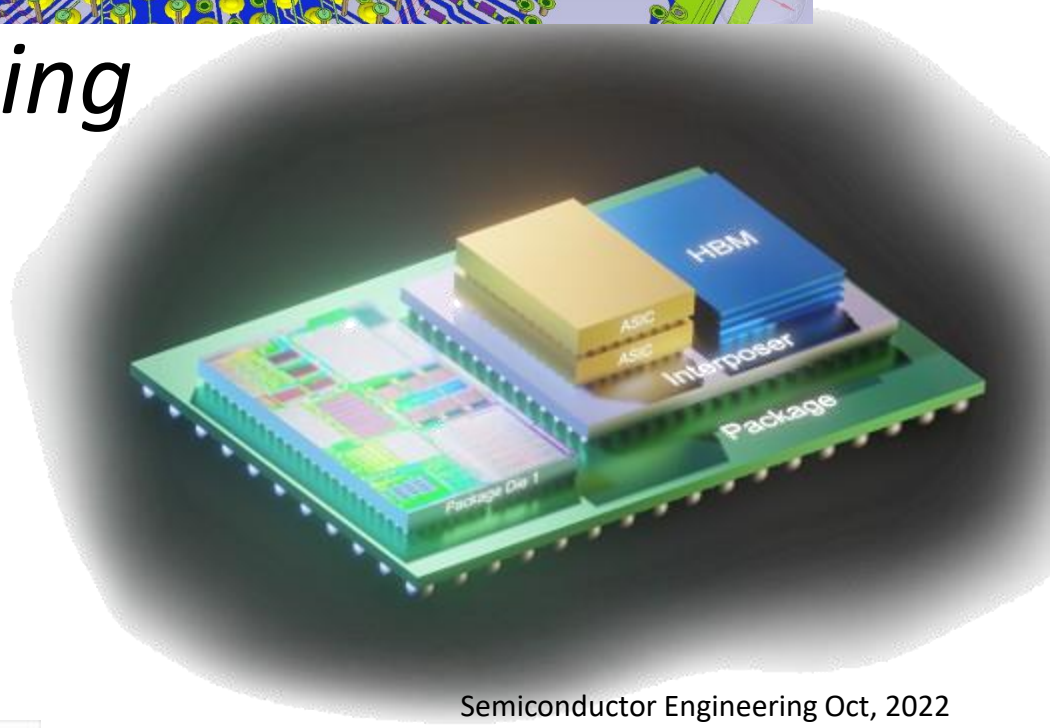
Co-Design and Multi-Physics

- Multi-Dimensional Tools
  - Scale
    - Nanometers to centimeters
  - Electrical
    - Power
    - Signal Integrity
  - Heat
  - Mechanical
    - CTE
    - Modulus
  - Cost
  - Photonics
  - MEMS
  - Liquids

Zuken



Forthcoming ADKs!

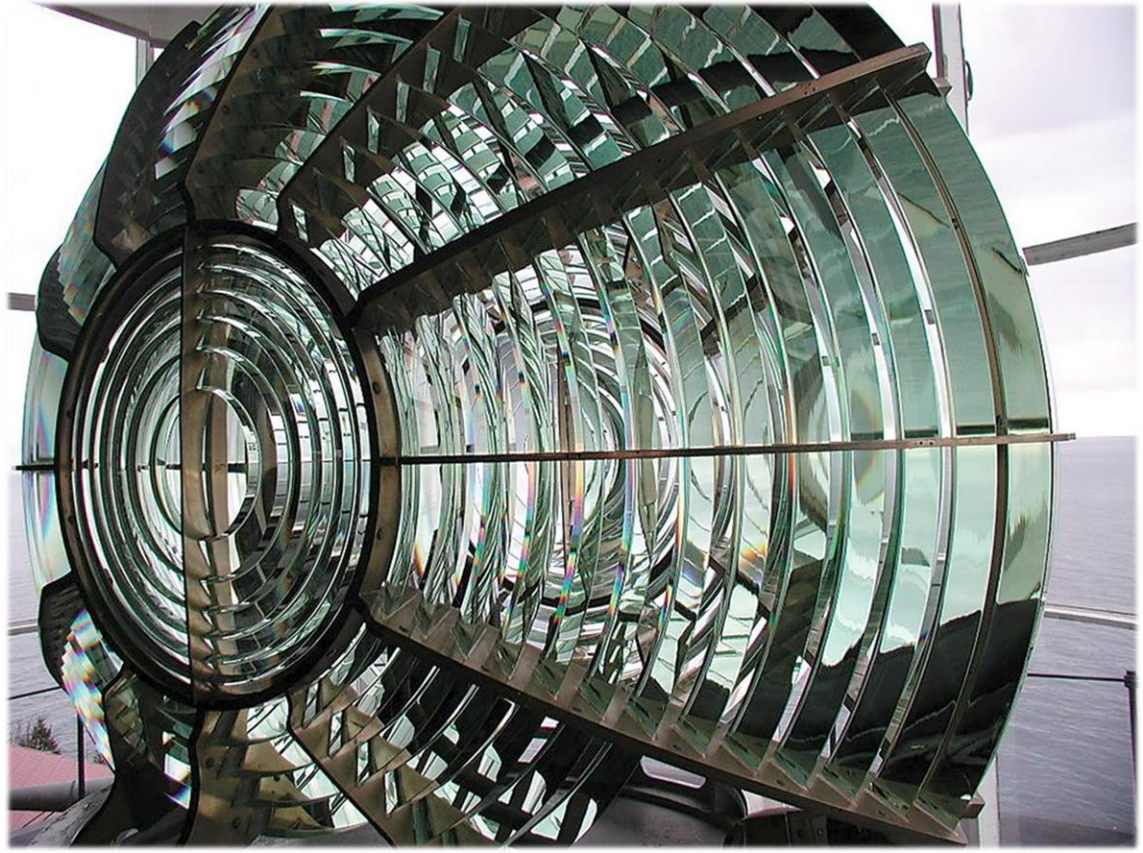


Unprecedented Complexity

Semiconductor Engineering Oct, 2022

A Change In Perspective Foundry 2.0

- A new focus on next generation semiconductors created by
  - Advanced Packaging
  - Additive Semiconductor Manufacturing
  - True heterogenous integration
  - Interconnect focused – all BEoL additive
    - Better ROI
    - Lower development costs
    - Lower CAPEX
  - Leveraging existing foundries
    - Split Fab
  - More Than Moore Technologies
    - IP Centric
    - Intrinsic value based – not cost of capital



Split Rock Lens – StackExchange

System Level Moore's Law