The Future of Electronics Packaging Is Chiplet Architecture

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***Abstract*—The transition from monolithic System-on-Chip (SoC) designs to chiplet-based architectures has redefined the landscape of advanced electronics packaging, driven by demands for increased functionality, heterogeneous integration, and improved performance per watt. Central to this shift is the development of high-density, low-latency interconnect technologies that can support multi-chiplet integration within a single package. Among these, hybrid bonding has emerged as a key assembly technique, offering superior electrical, thermal, and mechanical performance compared to conventional micro-bump and thermocompression bonding methods. Hybrid bonding enables direct copper-to-copper (Cu-Cu) and dielectric-to-dielectric interfaces between dies or chiplets at sub-10 µm pitches, dramatically increasing interconnect density while reducing parasitic resistance, capacitance, and interconnect latency. This paper serves as a technical roadmap and process assessment for the integration of hybrid bonding in fine pitch chiplet packaging.**

***Index Terms*—Chiplet, Hybrid Bonding, Cu-Cu Bonding, Advanced Packaging, Chiplet-to-wafer, Warpage, Alignment.**

I. INTRODUCTION

The rapid evolution of semiconductor technology has exposed the limitations of traditional monolithic SoC designs [1], [2]. As complexity increases and transistor scaling yields diminishing returns, the industry is transitioning toward chiplet-based architectures—modular systems composed of multiple smaller functional dies, or chiplets, fabricated independently and integrated within a single package [3], [4]. This disaggregation improves design flexibility, supports heterogeneous integration, and enhances scalability [5].

A key advantage of chiplet architecture is the ability to integrate logic, memory, analog, and I/O blocks developed at different process nodes. This approach enables the optimization of power, performance, and area (PPA) across functional domains, allowing the reuse of known-good dies (KGDs) and thereby reducing cost while improving yield. Such flexibility is particularly valuable in emerging applications, such as artificial intelligence (AI), data center computing, and high- bandwidth memory (HBM), where functional specialization and rapid iteration are critical [6].

However, effective chiplet integration requires interconnect technologies that support high density, low resistance and capacitance, as well as minimal thermal and mechanical stress. Conventional methods—such as micro-bump bonding and thermocompression bonding—face significant limitations at sub-10 µm pitches. These constraints have driven the emergence of hybrid bonding as a next-generation interconnect solution [7], [8]. As shown in Fig. 1, hybrid bonding technology, with its increasing market size and opportunities for innovation, enables direct Cu–Cu and dielectric-to-dielectric contact between dies without the need for solder or underfill. It eliminates intermediary layers, reduces interconnect height, minimizes parasitic effects, and improves thermal and mechanical integrity. These characteristics make hybrid bonding especially suitable for fine-pitch, high-performance chiplet systems [9], [10].

This paper examines the process architecture, integration flow, and fabrication challenges associated with hybrid bonding for chiplet-to-wafer (C2W) packaging. It also discusses defect mechanisms such as void formation, misalignment, and wafer warpage, along with recent advances in bonding materials, surface preparation, and standardization trends like Universal Chiplet Interconnect Express (UCIe), which are guiding the development of scalable, high-yield chiplet integration platforms.

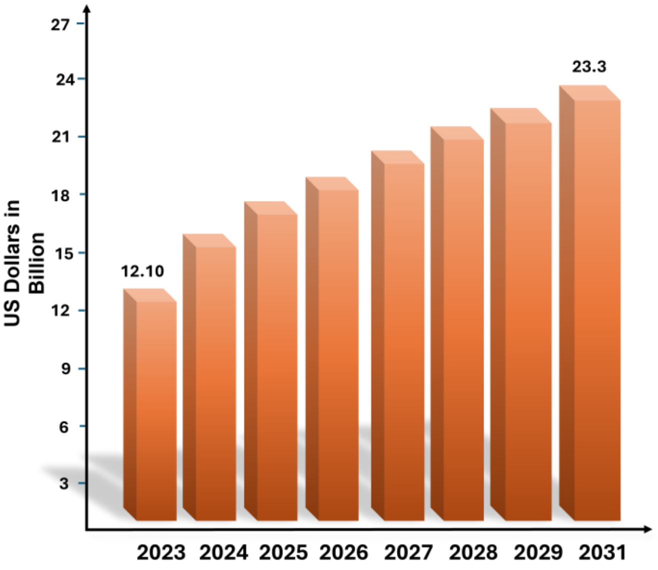

Fig. 1. Current State of Global Hybrid Bonding Technology Market [11]

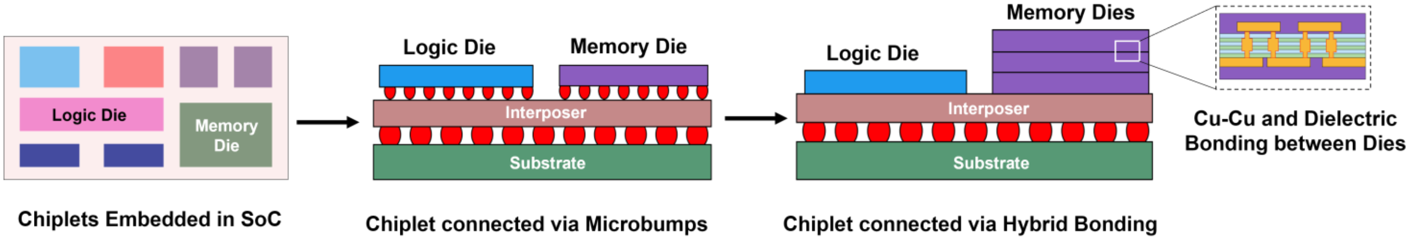

Fig. 2. Transition of Chiplet Architecture from SoC to 2.5D and 3D Advanced Packaging

II. HYBRID BONDING TECHNOLOGY: FUNDAMENTALS AND BENEFITS

As chiplet-based architecture has become the dominant integration model in advanced packaging, the need for interconnects that are ultra-dense, low-latency, and thermally efficient has intensified [3] as seen from the increasing trend towards miniaturization and compactness of the dies in Fig. 2. Hybrid bonding has emerged as a leading solution to meet these requirements, enabling fine-pitch die-to-die integration with strong electrical, mechanical, and thermal continuity through a co-optimized process flow.

Unlike thermocompression or micro-bump bonding, which rely on solder joints, epoxy underfills, and elevated bonding pressures, hybrid bonding forms direct Cu–Cu and dielectric-to-dielectric interfaces without the use of intermediary materials. This approach reduces the overall interconnect stack height, minimizes parasitic resistance and capacitance, and improves both mechanical integrity and thermal conduction. These characteristics are particularly beneficial in chiplet-based systems used for high-performance computing, AI accelerators, and HBM applications, where signal integrity, thermal reliability, and interconnect density are critical [12].

Table I compares key properties of hybrid bonding and conventional micro-bump bonding, including pitch scalability, stack height, thermal interface resistance, and current density handling [13].

Fig. 3 illustrates the hybrid bonding process flow. The integration sequence involves a tightly controlled set of steps designed to ensure reliable interface formation across both copper and dielectric surfaces.

III. HYBRID BONDING PROCESS INTEGRATION FLOW

Hybrid bonding begins with a series of tightly regulated process steps that integrate materials engineering, precision alignment, and surface conditioning to achieve robust interconnects at ultra-fine pitches. The overarching objective is to realize low-latency, high-yield, and reliable chiplet integration. Each stage of the bonding flow is instrumental in eliminating voids, enhancing mechanical stability, and mitigating risks associated with electromigration [21], [22]. As shown in this section, the hybrid bonding sequence typically comprises five critical phases: surface planarization, cleaning and surface activation, die alignment, low-temperature bonding, and post-bond annealing.

TABLE I
KEY PROPERTY DIFFERENCES BETWEEN HYBRID BONDING AND MICRO-BUMP BONDING

Property	**Hybrid Bonding**	**Micro-Bump Bonding**
Minimum Pitch	$<$10 µm [14]	$\geq$30 µm [15]
Interconnect Stack Height (Z-height)	$\leq$5 µm [10]	20–30 µm [16]
Contact Interface	Cu–Cu and oxide–oxide	Solder-based
Thermal Interface Resistance	$\sim$1.2 mm^2·K/W [17]	$\sim$8–15mm^2·K/W [18]
Current Density Handling	$>$8.9 MA/cm^2 [19]	$\sim$1.5–5 MA/cm^2 [20]

A. *Surface Planarization and Oxide CMP*

A reliable hybrid bond starts with achieving a uniformly planar surface. It is achieved through chemical mechanical planarization (CMP), which simultaneously levels the exposed copper pads and the surrounding dielectric layers [23]. Ensuring planarity at this step is essential for promoting full-area contact during bonding and avoiding the formation of localized voids or mechanical stress points [24]. To further improve dielectric uniformity and slurry selectivity during CMP, some process flows incorporate capping layers such as silicon nitride (SiN) or silicon dioxide (SiO_2) [25]. Additionally, since wafer bowing can compromise contact uniformity, warpage compensation techniques are often employed at this stage.

B. *Cleaning and Surface Activation*

Following planarization, the bonding surfaces are subjected to surface activation to ensure strong interfacial adhesion between the copper and dielectric layers. This critical step removes residual contaminants such as slurry particles and eliminates native copper oxides that may have formed during previous processing. In addition to cleaning, surface activation increases the surface energy of both materials, thereby enhancing wettability and enabling atomic-level bonding. These treatments are essential for achieving long-term mechanical integrity and electrical continuity at the bonded interface.

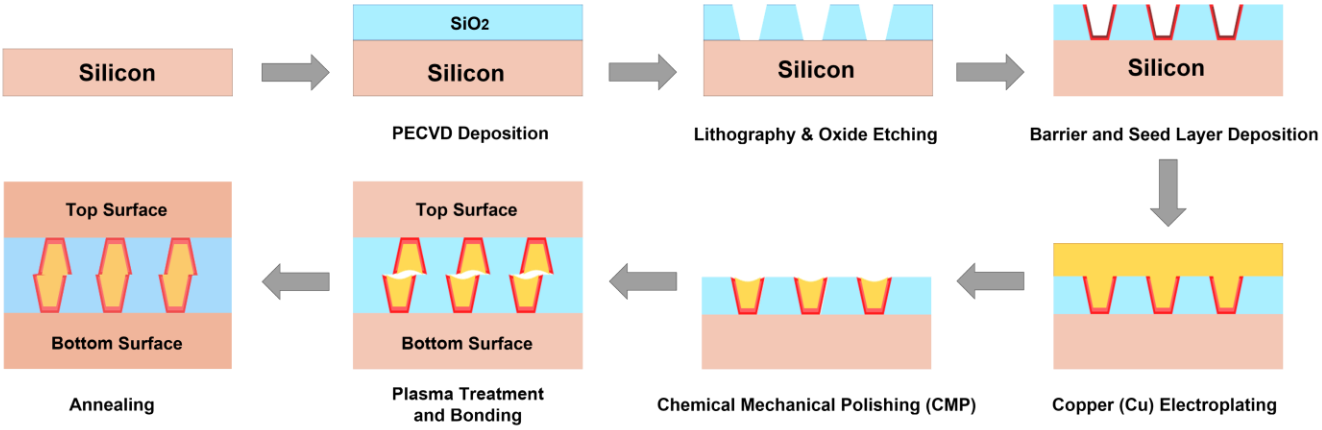

Fig. 3. Process Flow of Hybrid Bonding

C. *Die Alignment (C2W and W2W)*

Achieving accurate alignment is essential for realizing functional, fine-pitch interconnects in hybrid bonding. In wafer- to-wafer (W2W) configurations, the process relies on global wafer marks that guide stepper systems to achieve overlay accuracy better than 500 nm across the entire wafer surface. The inherent uniformity of whole wafers simplifies alignment and supports high-throughput batch processing.

In contrast, C2W bonding presents a more intricate set of challenges. Singulated dies often exhibit variations in thickness, warpage, and edge quality, making precise alignment more demanding. Each die must be individually picked and accurately placed onto the target wafer with sub-200 nm precision to ensure proper pad-to-pad overlap at pitches below 5 µm. To accomplish this, advanced placement systems leverage infrared and optical fiducial recognition to identify positional offsets, correct rotational deviations, and compensate for geometric distortion before bonding. Given the inherent variability between dies, pre-characterization of chiplet dimensions and topography is often required to ensure precise alignment and bonding integrity. A comparison of C2W and W2W bonding is shown in Table II.

D. *Low-Temperature Bonding*

Once alignment is complete, the top and bottom surfaces are brought into direct contact under carefully controlled pressure and at relatively low temperatures. The initial bonding occurs at the dielectric interface, where van der Waals or hydrogen bonds provide mechanical stabilization without the need for high-temperature processing. This low-temperature bonding strategy is particularly beneficial, as it minimizes thermomechanical stress and helps preserve the structural and electrical integrity of sensitive device layers within the chiplet stack.

E. *Post-Bond Annealing*

To complete the bonding process, a post-bond annealing step is carried out to strengthen the interconnect. During this thermal phase, solid-state diffusion and grain growth are initiated at the Cu–Cu interface, transforming the initial physical contact into a robust metallurgical bond. The annealing is typically performed at temperatures ranging from 200–300°C, with specific conditions determined by factors such as copper pad geometry, grain characteristics, and the composition of the surrounding dielectric stack.

In addition to enhancing copper bonding, the post-annealing phase plays a vital role in improving dielectric adhesion, relieving accumulated stress, and healing minor interfacial voids. Together, these improvements contribute to lower contact resistance, better thermal conductivity, and greater long-term reliability, particularly in environments subject to electromigration and repeated thermal cycling.

IV. ASSEMBLY SCENARIOS: C2W

The success of hybrid bonding in chiplet-based integration is closely tied to the choice of assembly configuration. Among the available strategies, C2W and W2W bonding are the two most widely adopted approaches. Although both methods rely on the exact core mechanism, establishing direct copper and dielectric interfaces, their implementation diverges significantly due to differences in die handling procedures, alignment accuracy requirements, and system-level integration constraints. These variations directly influence factors such as process yield, scalability, and design flexibility.

Selecting the most suitable bonding approach requires a comprehensive assessment of system performance goals, fabrication complexity, and architectural needs. For example, in C2W assembly, a pick-and-place system is used to position each die precisely on the wafer, utilizing alignment fiducials, as illustrated in Fig. 4.

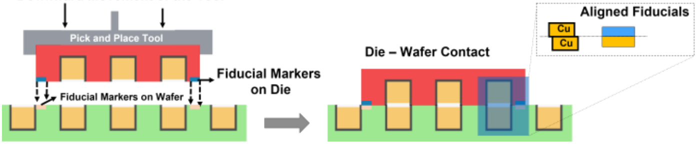

Fig. 4. Schematic of a Pick-and-Place tool positioning a chiplet on top of a Wafer

TABLE II
COMPARISON OF CHIP-TO-WAFER AND WAFER-TO-WAFER BONDING

Metric	**C2W Bonding**	**W2W Bonding**
Alignment Method	Sub-micron alignment via vision systems; adaptive placement of KGDs	Global wafer-level alignment using stepper systems or optical marks
Throughput	Moderate; limited by serial die placement and alignment overhead	High; entire wafer bonded in batch, suited for volume manufacturing
Yield Dependency	Favorable for heterogeneous integration; yield preserved by using only KGDs	Yield is sensitive to wafer-level uniformity; defects or non-uniformity
Die Uniformity Requirements	Critical: each die must meet planarity and thickness targets to ensure reliable interconnect formation	Important; global Wafer planarity managed via pre-bond CMP and thinning uniformity
Equipment Complexity	High; advanced pick-and-place tools with real-time metrology and surface correction	Moderate; streamlined equipment flow with fewer moving components
Application Examples	High-performance compute tiles, custom logic integration, AI/ML chiplet modules	HBM stacks, image sensor arrays, logic-memory vertical integration with high Wafer yield

This section highlights C2W bonding as the favored approach for achieving heterogeneous integration in advanced packaging. Its growing preference stems from the flexibility it offers in assembling known KGDs from diverse process nodes onto a common substrate. While W2W bonding is also relevant, its dependence on full-wafer integration poses limitations in terms of die reuse, component mixing, and design versatility, particularly when integrating dies fabricated using different technologies.

The comparative process variations between C2W and W2W bonding are visually summarized in Fig. 5, with key bonding and assembly parameters concisely presented in Table II.

A. C2W: Flexibility and Throughput Trade-offs

C2W hybrid bonding offers enhanced architectural and design flexibility by enabling the integration of individually tested known KGDs onto a processed wafer. This approach is particularly beneficial for heterogeneous systems, where chiplets may vary in size, function, or underlying process technology. For instance, a single package might incorporate logic dies fabricated at advanced nodes, memory dies from HBM stacks, and analog or RF tiles built on specialized process technologies—all bonded onto a common substrate.

However, this flexibility comes with a unique set of manufacturing challenges. Handling individual dies increases the risk of edge chipping, warpage, and dimensional inconsistencies. Each chiplet must be aligned with sub-micron accuracy, which requires the use of sophisticated pick-and-place equipment combined with high-precision optical alignment tools. Moreover, variations in die thickness and warpage can compromise overall planarity, making it necessary to tightly control die-to-wafer coplanarity to avoid voids or delamination during bonding. Despite these complexities, C2W bonding remains the method of choice for advanced system-in-package (SiP) designs where yield optimization, functional heterogeneity, and design customization are prioritized over sheer throughput.

V. KEY FABRICATION CHALLENGES

A. Pitch-Dependent Issues

The geometry of copper interconnects, particularly the pitch between adjacent pads, plays a critical role in determining the reliability of hybrid bonding. As the pitch scales down, the nature of potential failure mechanisms shifts noticeably. At larger pitches, bonding issues are typically dominated by topographical and mechanical factors. However, as the pitch decreases to sub-micron levels, atomic-scale material interactions become the primary concern. This transition in failure modes has a significant influence on the bonding behavior and a profound effect on the long-term reliability of the interconnects.

1) Large Pitch Regimes: Copper Dishing during CMP: When copper pad pitches exceed >10 μm, the broader Cu features present several challenges during the CMP process. One of the most prevalent issues is copper dishing—a phenomenon where copper is removed more aggressively than the surrounding dielectric material. This results in recessed copper pads, which in turn reduce the effective contact area at the Cu–Cu interface, as illustrated in Fig. 6.

These dished features disrupt uniform bonding pressure, particularly at the center of each pad, where the contact height is diminished. This unevenness can hinder proper bond closure, elevate parasitic resistance and inductance, and create localized Joule heating, especially under high current densities. In C2W bonding configurations, such non-uniform dishing can lead to inconsistent bond strength and introduce alignment complications [26]. For chiplets with recessed or topographically uneven surfaces, this often results in only partial area contact, thereby degrading electrical connectivity and thermal performance.

2) Small Pitch Regimes: Intra-Pad Uniformity and Copper Corrosion: As interconnect pitches shrink into the sub-10 micron range (<10 μm) and the experimental range (<1 μm), the nature of bonding challenges shifts from geometric to material-centric concerns [27]. Although narrow copper

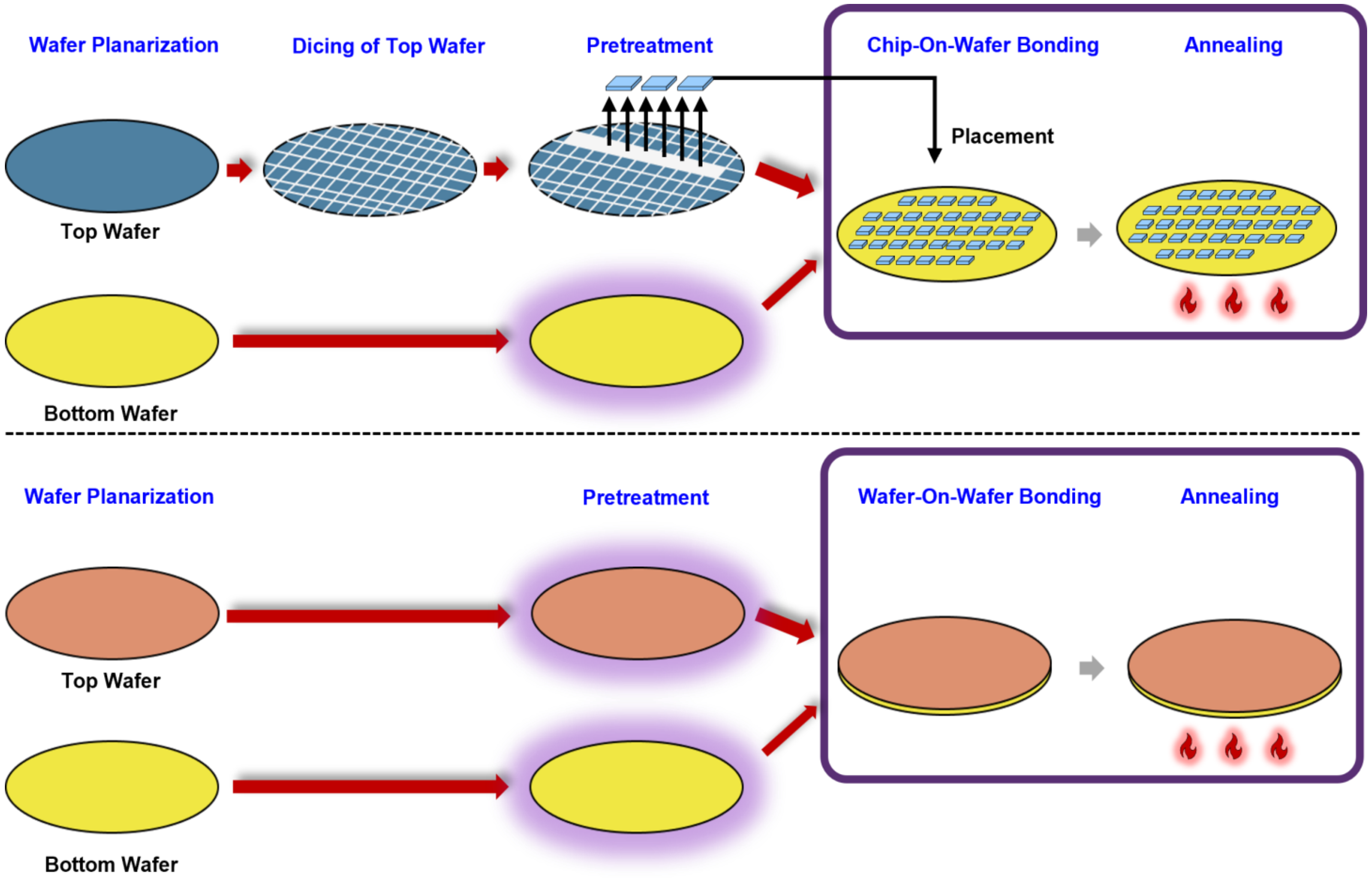

Fig. 5. CoW and WoW Processes

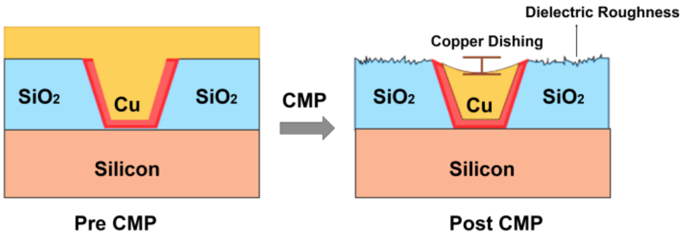

Fig. 6. Individual Cu Pad level observation of Dishing and Dielectric roughness induced by Improper CMP Process

features are less susceptible to dishing, they become increasingly sensitive to factors such as micro-scale surface roughness, contamination, and oxidation [28].

One of the key issues at this scale is intra-pad height variation, often arising from grain boundary irregularities or incomplete CMP. Such variations can disrupt full-area contact during bonding, leading to elevated contact resistance and localized mechanical stress. Additionally, copper surfaces are susceptible to corrosion between the CMP and bonding steps. Even brief exposure to ambient conditions can result in the formation of thin copper oxide layers, which act as diffusion barriers during post-bond annealing. These oxides hinder effective Cu–Cu bonding and may lead to voids or parasitic capacitive coupling when surrounded by dielectric discontinuities. Fig. 7 illustrates examples of these sensitive processing defects that can emerge during sub-micron pitch hybrid bonding.

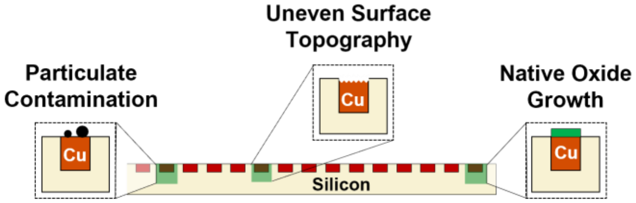

Fig. 7. Defects Observed at Sub-Micron Pitches

B. Bonding Defects

Since hybrid bonding eliminates the use of solder and underfill, the integrity of the direct contact between copper and dielectric surfaces becomes paramount. Ensuring high-quality contact at this stage is, therefore, essential to maintain continuity, minimize resistance, and uphold long-term reliability.

1) Voids: Voids represent one of the most common and damaging defects encountered in hybrid bonding. They typically form when air or gas becomes trapped between the bonding surfaces during die placement. Even small voids at the Cu–Cu interface can result in open circuits or introduce high-resistance pathways. When present in dielectric regions, voids reduce both thermal conductivity and dielectric strength, thereby posing significant reliability concerns—particularly under thermal cycling conditions.

In C2W bonding, void formation is often triggered by asymmetric die contact, where one edge of the chiplet makes contact before the rest of the die settles. This uneven touchdown disrupts the bond wave propagation and creates pockets of trapped air. The issue is further exacerbated in thinner dies, which are more prone to flexing and non-uniform contact. These types of defects are commonly detected using scanning acoustic microscopy (SAM), which offers sub-micron resolution to locate and characterize voids across the bonded interface [29].

2) Warpage: Warpage of the wafer or die can significantly compromise the uniformity of the bonding interface, ultimately leading to reduced yield. This deformation is often introduced during earlier process steps, such as Wafer thinning, oxide deposition, or metal patterning, where residual stress accumulates. Additionally, mismatches in the coefficients of thermal expansion (CTE) between stacked layers can intensify bowing across the structure.

In C2W bonding, thin chiplets—particularly those less than 50 µm thick—behave like flexible membranes and are especially susceptible to warpage. This deformation results in uneven contact pressure during bonding, misalignment at the Cu–Cu interface, and, in some cases, lifting at the chiplet edges after placement. Warped dies are also more vulnerable to delamination when subjected to thermal cycling, especially if differential expansion persists after bonding is completed. For this reason, precise warpage control is critical—not only to ensure high-quality bonding but also to maintain the long- term reliability of the package.

Fig. 8 illustrates various forms of wafer warpage, including the deformation of both wafers and dies after bonding.

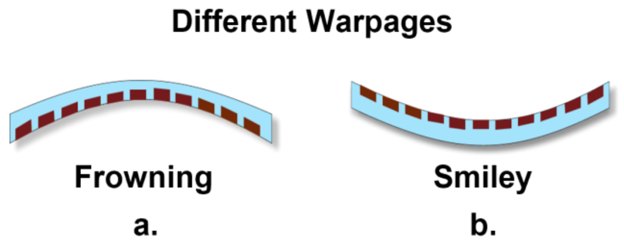

Fig. 8. a. Concave (frowning) Warpage b. Convex (Smiley) Warpage

C. C2W-Specific Challenges

In C2W bonding flows, each die is bonded individually, treating every attachment as a discrete event. Unlike W2W bonding, which benefits from the symmetry and uniformity of full-wafer processing, C2W must accommodate die-specific inconsistencies in planarity, internal stress, and geometric dimensions.

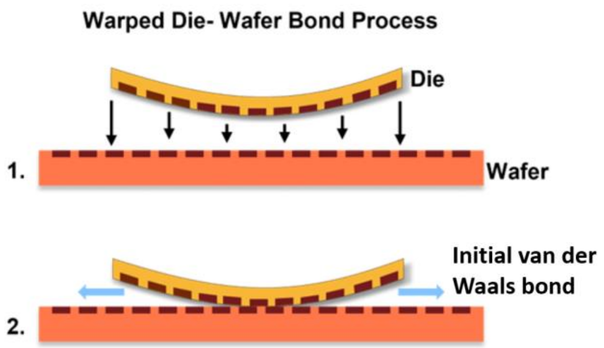

Fig. 9. Warped Die-Wafer Bonding Process showing a smiley thin die wafer bonding with a flat wafer by the initial van der Waals bonding forces

1) Edge Effects in Die Placement: Chiplets positioned near the wafer edge are more prone to alignment errors, bonding defects, and distortion following post-bond annealing [30]. These issues stem from local non-uniformities that are inherent to edge regions, such as CMP edge exclusion zones, residual stress introduced during film deposition, and uneven chuck pressure during processing. Furthermore, thermal gradients during annealing are typically more pronounced at the wafer periphery. This intensified heating leads to greater expansion mismatches, which in turn raise the risk of partial delamination and compromises the mechanical integrity of edge-located dies.

2) Precision in Die Placement: The accuracy of die placement plays a critical role in determining the overall quality of hybrid bonding. Even slight misalignments in X/Y translation, θ rotation, or Z-height can result in incomplete pad contact, short circuits, or deformation of sensitive interconnect structures. Achieving sub-micron placement precision is essential and relies on advanced machine vision systems, closed-loop feedback control, and real-time alignment verification.

However, several factors can introduce variability during the placement process. Collet wear, mechanical tool drift, and thermal expansion can all contribute to positional errors. Moreover, thin chiplets are particularly vulnerable to flexing when handled by vacuum-based collet systems, often resulting in a slightly curved profile that hinders coplanar landing. These distortions lead to reduced contact uniformity and increase the risk of mechanical or electrical failure, as even minor misalignments between copper pads can elevate insertion losses [31].

3) Recess Control and Pad Height Variation: In C2W bonding, due to the inconsistent CMP, post-cleaning processes, there is often noticeable variability in copper pad height and oxide surface uniformity from chiplet to chiplet. These inconsistencies are commonly caused by localized CMP dishing or over-etching, which can lead to copper recess. When this recess exceeds just a few nanometers, the bonding force shifts from the intended copper pad to the surrounding oxide; this misdistribution weakens the Cu–Cu interface and can result in incomplete or unreliable bonds, compromising the electrical and mechanical integrity of the interconnect. As shown in Fig. 9, after bonding the warped die to a flat wafer, pad height variation and localized recesses may cause the die-wafer attachment to remain warped if these imperfections aren't carefully addressed during the process.

4) Surface Cleanliness and Particle Control: Maintaining a clean bonding surface is essential for ensuring the reliability of C2W hybrid bonding. Unlike whole wafers, individual chiplets are more vulnerable to contamination during critical steps such as singulation, inspection, and placement. The dicing process can generate particulates that settle on copper pads or accumulate in the bonding chuck. Additionally, organic residues or plasma byproducts from earlier processing stages can interfere with adhesion or react during annealing, forming insulating, carbon-rich films that hinder bond quality [32]. As illustrated in Fig. 10, inadequate surface cleanliness can lead to contamination on the surface, resulting in unwanted air gaps between the die and the Wafer.

Because chiplets cannot undergo batch-level cleaning like whole wafers, in-line cleaning procedures must be implemented carefully. These processes must strike a balance between the effective removal of contaminants and the preservation of both copper pad and dielectric surface integrity.

Fig. 10. a. Close View of contamination on top of Cu Pad post CMP and Plasma Cleaning. b. Microscopic View of Air gaps created by the contaminated particle on the post-bonding interface

5) Post-Bond Alignment Drift: Following the bonding process, chiplets may experience alignment drift caused by die relaxation or thermomechanical mismatch between the chiplet and the substrate. The compressive stress applied during bonding can be partially released after placement, resulting in subtle positional shifts. This effect is often intensified during post-bond annealing, especially when there is a mismatch in the CTE between the materials, leading to nonlinear overlay distortion across the die.

For large area chiplets, this drift can vary spatially, introducing alignment errors even when the corner fiducials appear properly registered. These misalignments are typically more pronounced near the wafer perimeter, where registration accuracy tends to degrade. Detecting and quantifying such distortions requires precise metrology tools, including infrared and X-ray imaging systems, to assess their impact on routing precision and downstream electrical testing. As depicted in Fig. 11, even fiducial-based alignment systems can fall short in compensating for post-placement drift, particularly in edge regions of the wafer.

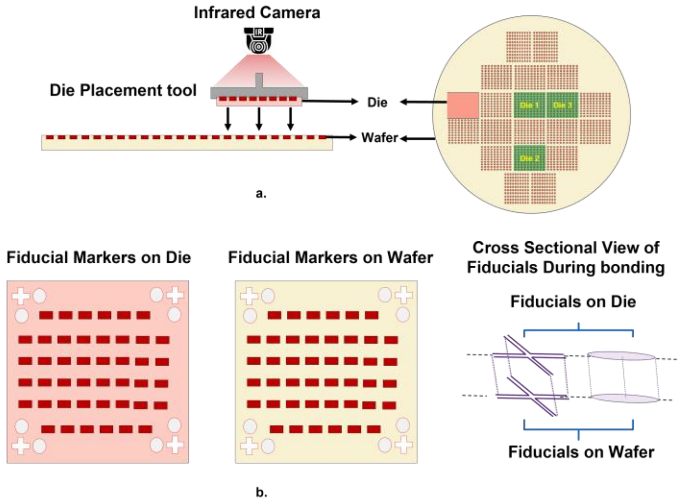

Fig. 11. Chiplet positioning on top of Wafer as per precise Fiducial Alignment, Extension of Fig. 4

6) Chiplet-Level Distortion Through Die: Chiplet deformation can arise from thermal, mechanical, or process-induced stresses, subtly altering the die shape either during or after bonding. Although these distortions are often difficult to detect visually, they can significantly impact alignment precision and compromise the reliability of interconnects. Such deformations typically originate from stress gradients introduced during upstream steps like wafer thinning, etching, or die mounting, and are further aggravated by non-uniform bonding pressure or improper thermal ramp rates [33].

In the case of large area chiplets, these distortions can exceed several hundred nanometers, causing internal misalignment across the die. To address this, metrology techniques employing in-die fiducial arrays are used to map the extent and nature of the deformation. These insights allow process engineers to fine-tune bonding pressure distributions and support mechanisms, thereby minimizing geometric relaxation and preserving die integrity.

VI. RECENT DEVELOPMENTS TOWARDS SOLVING THE CHALLENGES

Achieving scalable and reliable hybrid bonding in chiplet-based packaging requires ongoing advancements in process control and precision of integration. As interconnect pitches continue to shrink below 10 µm and chiplet architectures, grow more intricate, even slight variations can result in substantial yield losses and degraded performance. These challenges have driven the development of targeted solutions aimed at addressing key issues such as void formation, surface planarity disruption, alignment errors, and mechanical instability [28]. This section explores the most significant innovations that are enabling hybrid bonding to evolve toward high-volume manufacturability for next-generation fine-pitch systems.

A. Surface Planarization and Bond Interface Preparation

Once the CMP process is completed, the exposed bonding interfaces become highly susceptible to surface oxidation and mechanical damage. To maintain surface integrity during subsequent steps, protective layers—applied via spin coating or vapor deposition—are now commonly used to shield both copper and dielectric regions [34]– [36]. These protective coatings act as physical barriers, preventing the formation of native copper oxides and reducing the risk of surface abrasion during handling. The result is a cleaner, more uniform interface that supports improved Cu–Cu contact and enhanced dielectric continuity during bonding.

Recent advancements in this area demonstrated the integration of an inorganic protective layer into the C2W hybrid bonding workflow. This innovation significantly reduced surface contamination, resulting in a lower incidence of voids and improved chiplet overlay accuracy across the wafer [37].

B. Adhesive Layer Integration for Void Mitigation

To combat void formation, adhesive materials with tailored viscosity and curing profiles are applied after cleaning. These adhesives conformally fill micro-trenches and residual surface roughness, improving bond-line uniformity. In addition to smoothing the interface, the adhesive layer helps absorb mechanical stress during thermal cycling, thereby reducing the risk of interfacial delamination [38].

C. Misalignment Detection and Correction Techniques

Misalignment of chiplets—often caused by die warpage or stress introduced during dicing—remains a persistent challenge in C2W bonding workflows [39]. To address this issue, advanced alignment systems now incorporate real-time imaging and distortion mapping into the placement process. As shown in Fig. 12, fiducial-based systems equipped with infrared and optical cameras detect chiplet-scale scaling errors. These inputs are processed by software algorithms capable of executing sub-micron corrections in both rotational and translational directions [32]. This combination significantly improves overlay accuracy across the wafer and strengthens both electrical yield and mechanical coupling in high-density interconnect regions.

Intel presented a notable industry advancement in 2022, where a water dispense technique combined with tailored surface preparation was employed to correct misalignment during C2W assembly. This method demonstrated highly accurate placement, with at least 48% of dies aligning within 200 nm and over 70% achieving alignment better than 500 nm [40].

D. Control of Chiplet Bending During Attachment

Thin chiplets—particularly those less than 50 µm thick—are especially prone to bending during the handling process, which can result in uneven contact and trapped air at the bonding interface. To address this, modern bonding platforms are equipped with precision-controlled heads that gently and uniformly place the die across the die surface. This approach enables a consistent and well-regulated bonding process. Additionally, bond wave progression is carefully controlled, allowing the interface to close from the center outward in a deliberate pattern that minimizes the risk of air entrapment.

Complementing these efforts, thermally stable chucks and pressure-controlled chambers are employed to reduce chiplet flexure and help maintain a flat, defect-free bond line. Recently, a new solution was proposed that involves the use of Inter-die Gap Fill (IDGF) materials to mitigate wafer bowing further. By optimizing the thickness and stress profile of dielectric films, along with fine-tuning the copper percentage in the stack, this method showed promise in improving overall bonding uniformity [39], [41].

E. Carrier-Based and Organic Layer Management

Temporary carriers—typically made of glass or silicon—are widely used to provide mechanical support for thin wafers during thinning and bonding operations. Glass carriers offer the added advantage of enabling through- carrier alignment due to their transparency to infrared light. The process of attaching wafers to these carriers involves spin- coated adhesives, and managing these adhesives properly is critical to overall bonding success [38].

A uniform adhesive coating ensures consistent support across the wafer, while residue-free removal is crucial to prevent warpage and avoid scaling distortions during subsequent steps. Recent process improvements now focus on optimizing solvent bake conditions, maintaining adhesive layer uniformity, and implementing controlled debonding techniques—all of which contribute to preserving surface flatness and achieving precise alignment throughout the bonding workflow.

F. CMP Uniformity Control

Local non-uniformities during the CMP process—arising from uneven pad wear, inconsistent slurry distribution, or pressure fluctuations—can result in height variations that negatively affect bonding quality. These disparities lead to non-uniform copper and oxide surfaces, which in turn increase the risk of bond gaps and electrical shorts.

To overcome these challenges, modern CMP systems have adopted advanced control mechanisms, including zonal pressure feedback and real-time endpoint detection. These technologies dynamically adjust material removal rates across different wafer regions, helping to maintain uniform copper pad height and oxide thickness. Such refinements play a crucial role in enhancing bonding consistency and minimizing the likelihood of interconnect defects [25].

G. Vacuum-Controlled Bonding Environments

Performing the bonding process under vacuum conditions significantly enhances interface quality by eliminating trapped air, moisture, and volatile residues. Vacuum bonding chambers also promote smoother bond wave propagation by minimizing the aerodynamic resistance caused by displaced air during die contact.

In addition to the benefits of vacuum, the use of inert or reducing atmospheres within the chamber helps suppress copper oxidation, thereby maintaining a clean and active Cu–Cu

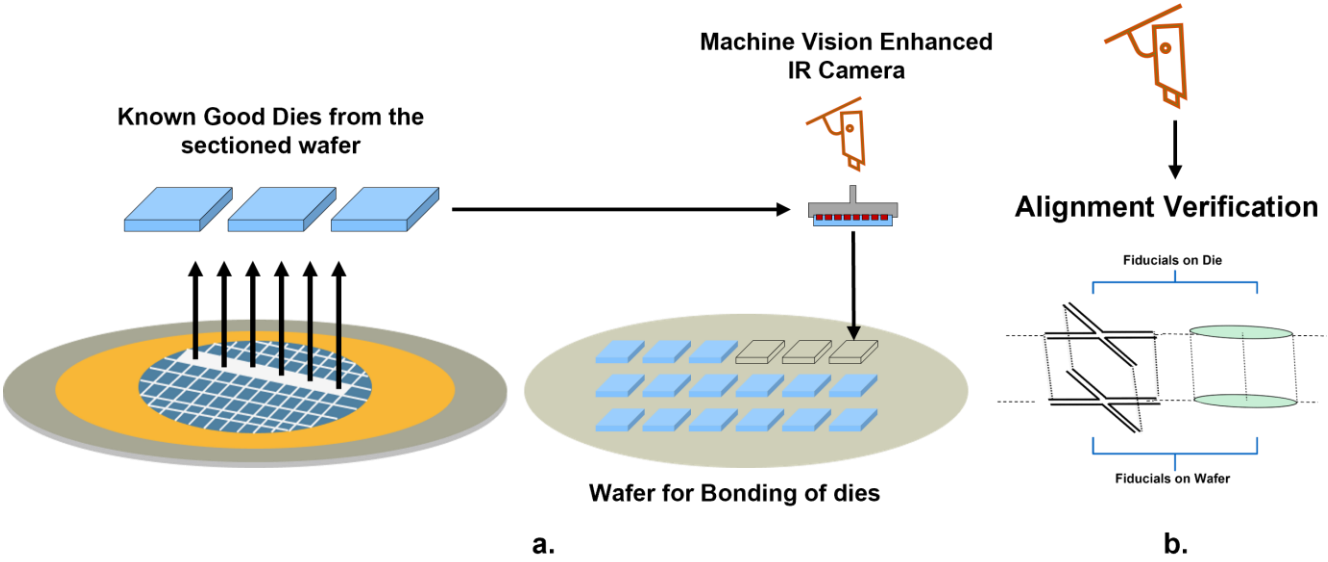

Fig. 12. a. Removal of Dies from the sectioned Wafer and placement on the new Wafer for CoW Integration. b. Machine vision enhanced IR Camera for Ensuring and Verifying a Precise Fiducial alignment

interface. These combined effects result in stronger bonds, fewer voids, and improved consistency in both electrical and thermal performance across the bonded structure [30].

H. AI/ML for Defect Prediction and Process Optimization

Machine learning is rapidly becoming a transformative tool for implementing predictive control in hybrid bonding processes. By analyzing real-time process data—such as alignment metrics, CMP parameters, surface topography, and defect density—AI models can detect early signs of failure and recommend timely corrective actions [42]. These systems adapt continuously, learning from equipment behavior and metrology feedback to fine-tune critical process parameters, including bonding pressure, temperature profiles, and cleaning protocols [43], [44].

Beyond predictive capabilities, machine learning also plays a key role in accelerating defect classification. By leveraging data from SAM, scanning electron microscopy (SEM), and optical imaging, AI algorithms facilitate faster root-cause analysis and tighter feedback loops. This integration significantly enhances yield and process stability at scale [45], [46].

VII. FUTURE OUTLOOK

The transition to hybrid bonding represents not just an evolutionary step in advanced packaging, but a foundational shift in how semiconductor integration will be structured in the coming decades [47], [48], [49], [50]. As monolithic SoC scaling faces cost and yield constraints, chiplet-based architectures—enabled by high-density interconnects—are redefining system design. The modularity provided by chiplets, combined with the fine-pitch capabilities of hybrid bonding, is setting a new standard for heterogeneous integration [13].

One of the most impactful developments driving this shift is the growing adoption of the Unified Chiplet Interconnect Express (UCIe) standard. UCIe defines a unified physical, electrical, and protocol-level interface for die-to-die communication, simplifying chiplet integration across vendors and process technologies. At the core of UCIe's physical layer is a requirement for low-latency, high-bandwidth interconnects at fine pitches—typically targeting <10 µm. Hybrid bonding is well positioned to meet and extend this requirement.

Unlike micro bump-based approaches, hybrid bonding enables highly planar, low-parasitic metallurgical connections that support low inter-die skew and uniform impedance, both of which are essential for UCIe compliance. It not only supports the standard but also extends its performance potential into sub-5 m pitch regimes, opening the door for more compact and power-efficient designs.

To enable this integration path, foundries are developing UCIe-compliant process design kits (PDKs) that include hybrid bonding modules optimized for thermal, power, and yield-aware floor planning. This alignment of standardized interconnect protocols with advanced packaging technologies signals a robust and scalable future for chiplet-based systems.

Continued improvements in bonding tool precision, surface preparation, and post-bond metrology will be crucial for scaling hybrid bonding to volume production. These advancements will play a key role in unlocking modular integration across a wide range of applications, including AI accelerators, data center computing, mobile SoCs, and other performance-critical domains.

VIII. CONCLUSION

The transition from monolithic SoC integration to modular chiplet-based architecture has fundamentally reshaped the landscape of advanced electronics packaging. At the core of this shift is hybrid bonding—a technology that meets the demanding electrical, mechanical, and thermal requirements of fine-pitch, low-latency inter-chip communication. This paper has outlined the key principles, integration flows, and fabrication challenges of hybrid bonding in die-to-wafer implementations. We have also highlighted recent process innovations that are pushing technology closer to high- volume production. Looking ahead, the future of hybrid bonding lies in its evolution toward bumpless, pitch-agnostic interconnects and native compatibility with open standards, such as UCIe and their inspection methodologies, integrating AI-integrated defect detection, multi-modal integration, non- destructive evaluation using Optical, X-ray, and SAM, and fine-tuning their models for future sub-10 µm and experimental sub-1 µm pitches. As industry converges on modular, heterogeneous platforms, hybrid bonding will continue to be a foundational enabler, shaping how systems are designed across materials, processes, and architectural boundaries.

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